AT5 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1
PAG 13,14
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 13,14
DDRII 533,667 MHz

PCI-Express 16X

NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA
PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON
PAG 26

TV_OUT
CRT_OUT
LVDS(2 Channel)

CRT/S-VIDEO
PAG 25

Panel Connector
15" / 17" PAG 26

Cable Docking
PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

DMI LINK

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

USB2.0

5 — **Bluetooth** PAG 35
0,1,2 — **USB2.0 I/O Ports X3** PAG 32
3 — **Camera X1** PAG 32
4,6,7 — **Mini PCI-E Card x1**
Express Card x1
Cable Docking x1

PCI BUS / 33MHz
PCI-E
Azalia

Option for 17" only
SATA - HDD PAG 35
SATA2

SATA - HDD PAG 32
SATA0 150MB

PATA- CD-ROM PAG 32
PATA (66/100/133)

LPC

Realtek
ALC 268
PAG 29

Two-element microphone PAG 29

Audio Jacks (Phone/ MIC) PAG 29

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 39

LAN
Realtek PCIE-LAN
RTL8101E/8111B
10/100/GagaLAN
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 27,28

SIM CARD PAG 32

RJ45 PAG 33

IEEE1394 CONN PAG 28

Memory CardReader PAG 27

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

Keyboard Touch Pad PAG 36

CIR PAG 36

Capacitive Sense SW PAG 36

X-Bus

FAN PAG 38

Flash PAG 37

SPI PAG 37

AUDIO Amplifier PAG 30

Jack to Speaker PAG 30

MDC DAA SI3080 PAG 31

MODEM RJ 11 PAG 33

SYSTEM CHARGER(MAX8724) PAG 41

SYSTEM POWER MAX8778 PAG 42

DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 46

VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 43

VGACORE(1.025V)MAX1992 PAG 45

CPU CORE MAX8771 PAG 44

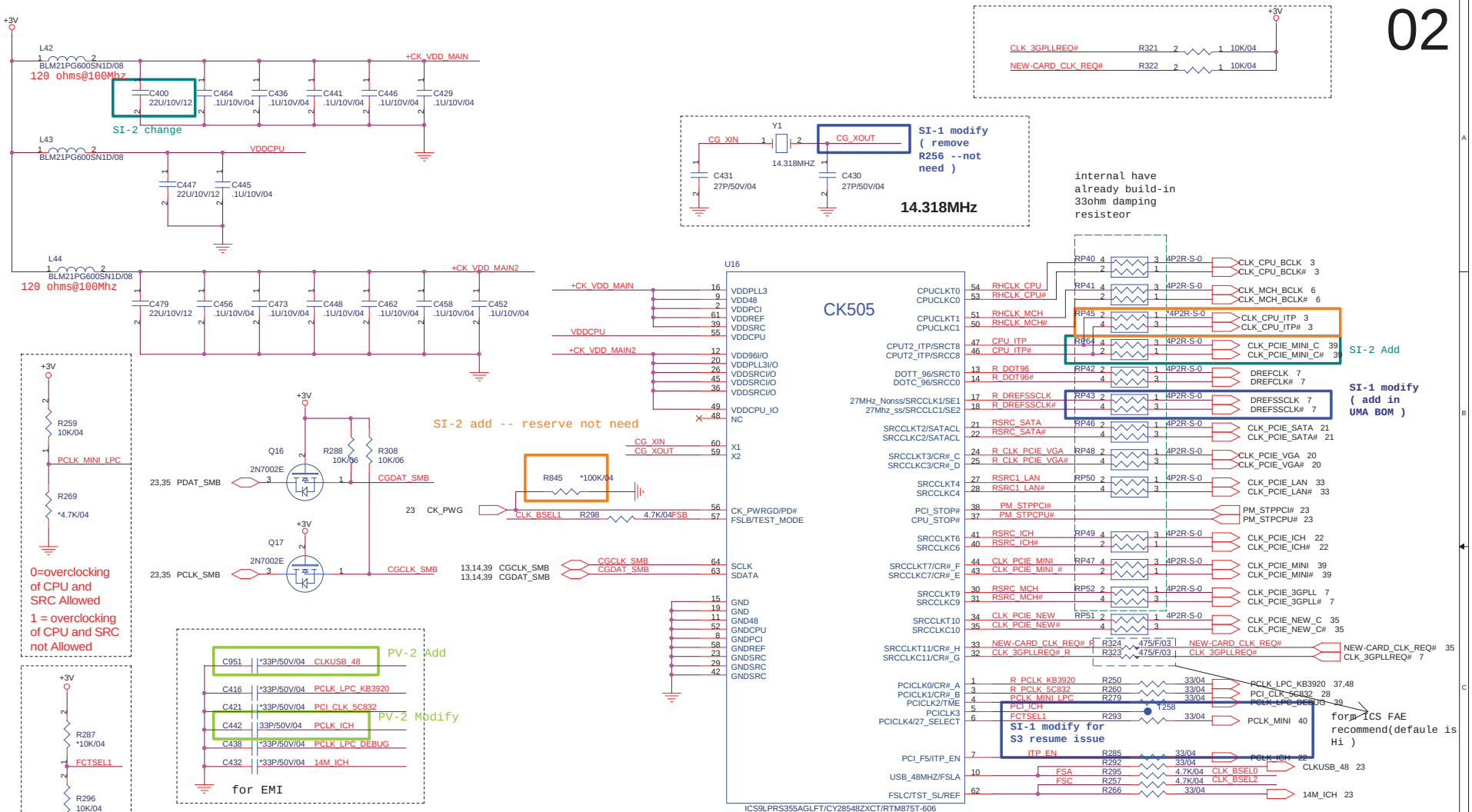
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT5
Quanta Computer Inc.

NB5/RD1/HW2

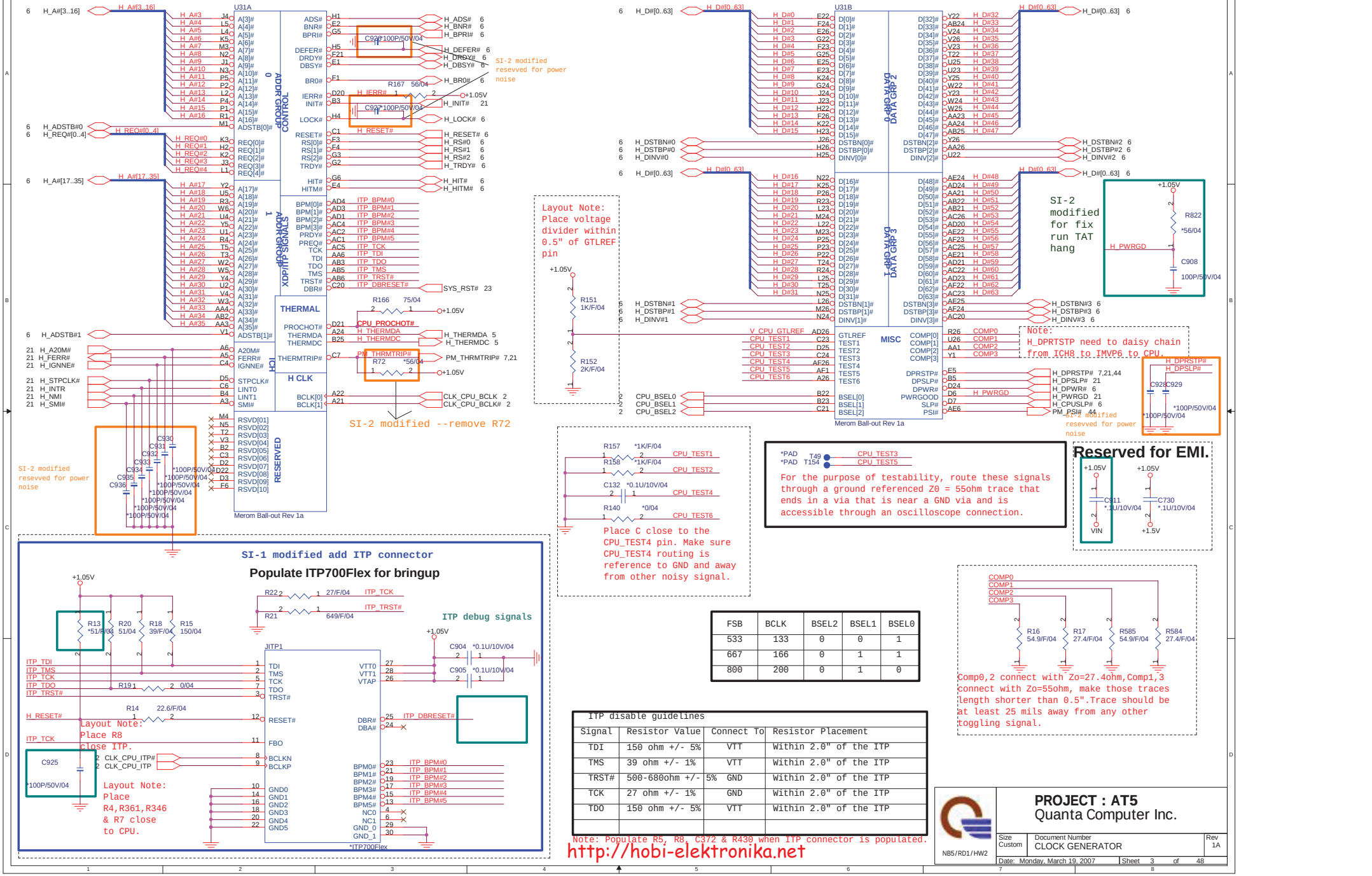
Size: Custom | Document Number: BLOCK DIAGRAM | Rev: 1A

Date: Monday, March 19, 2007 | Sheet 1 of 48



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

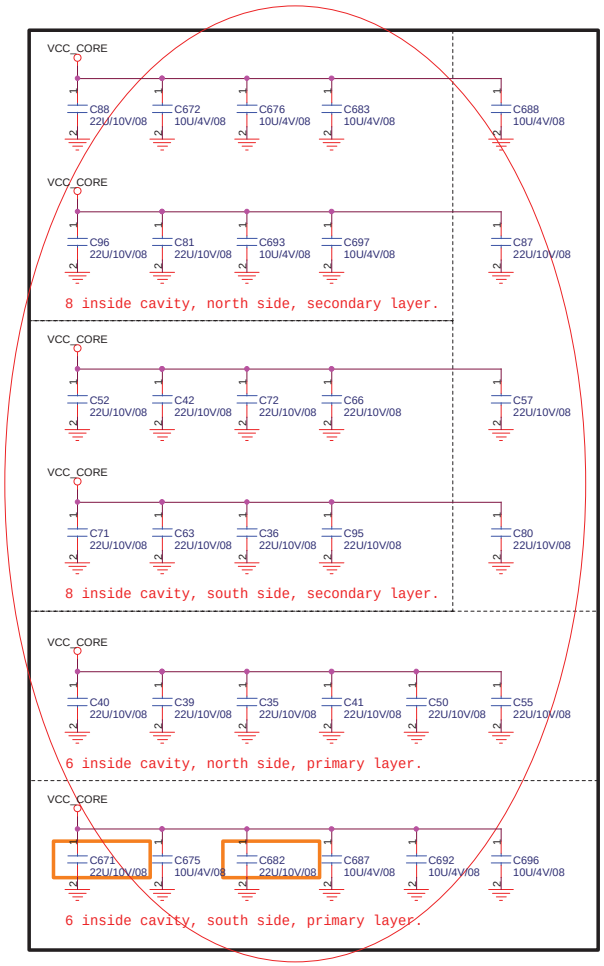
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

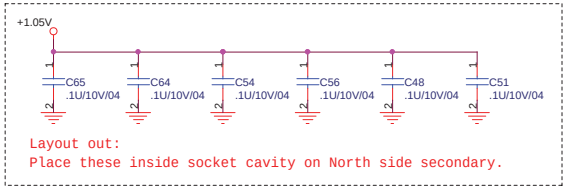
NB5/RD1/HW2

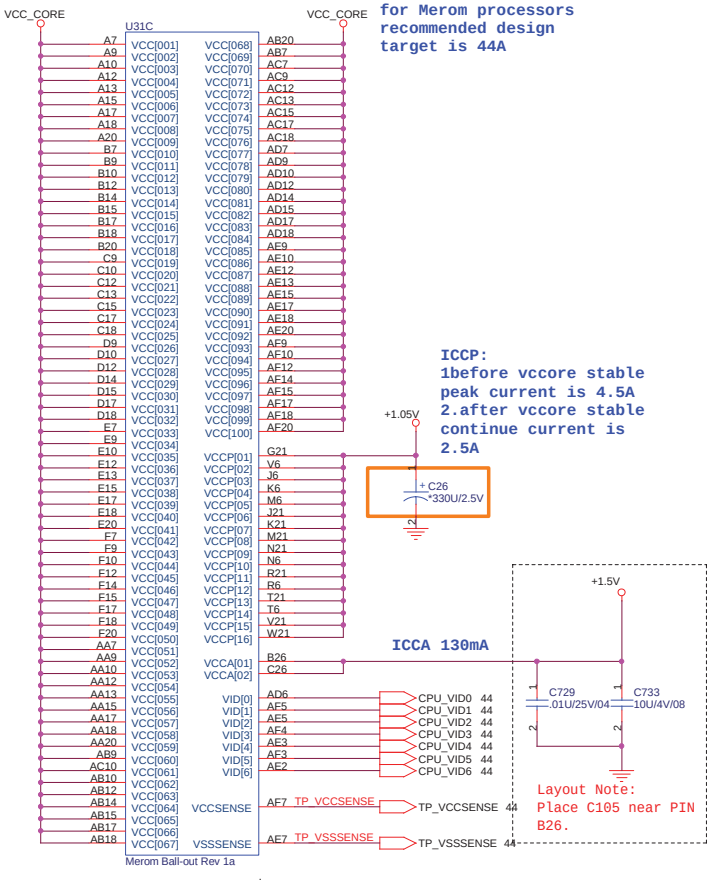
PROJECT : AT5
Quanta Computer Inc.

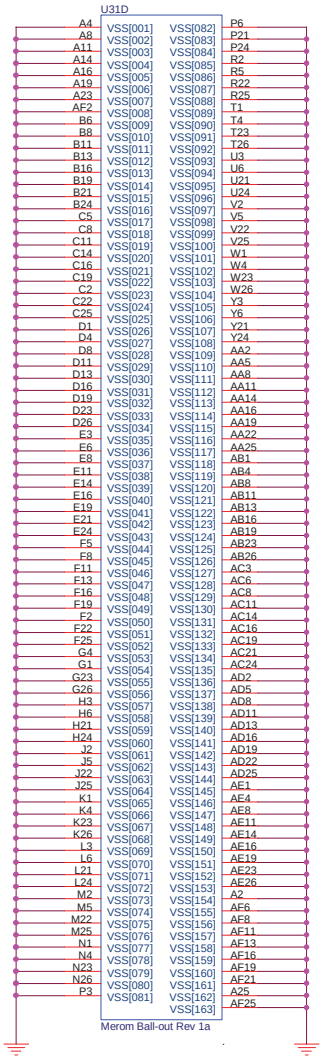
Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Monday, March 19, 2007 | Sheet 3 of 48







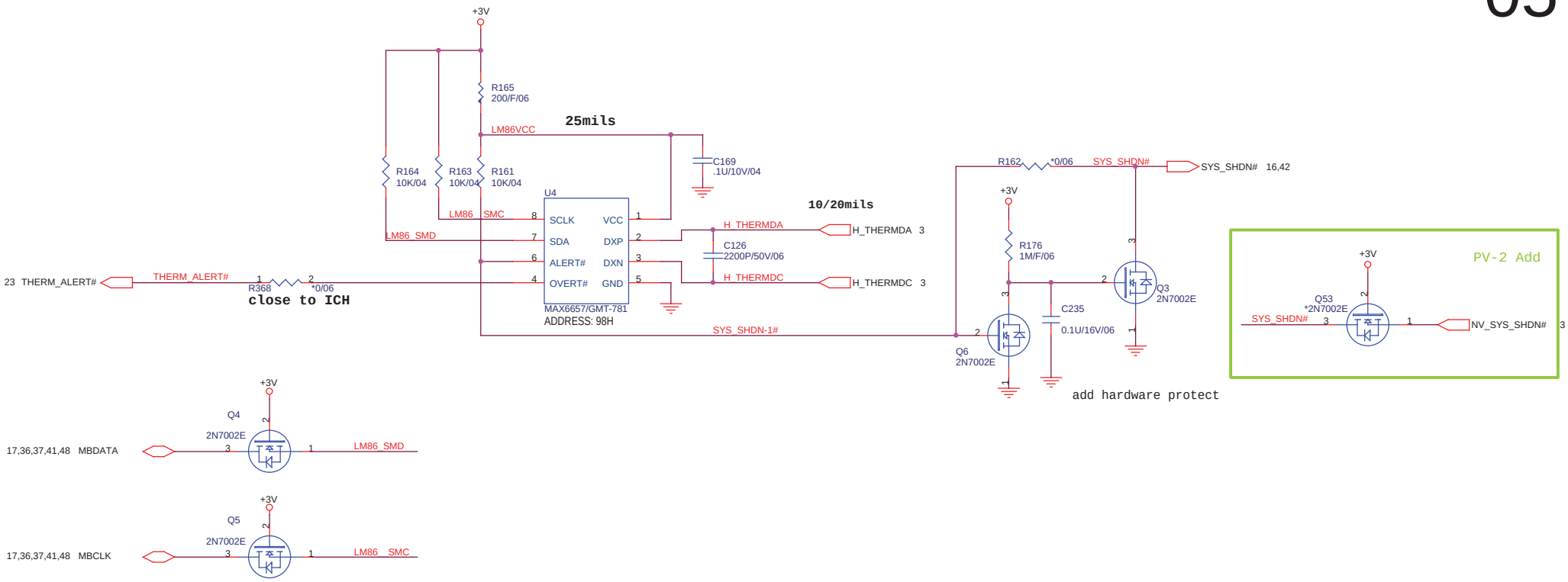


PROJECT : AT5
Quanta Computer Inc.

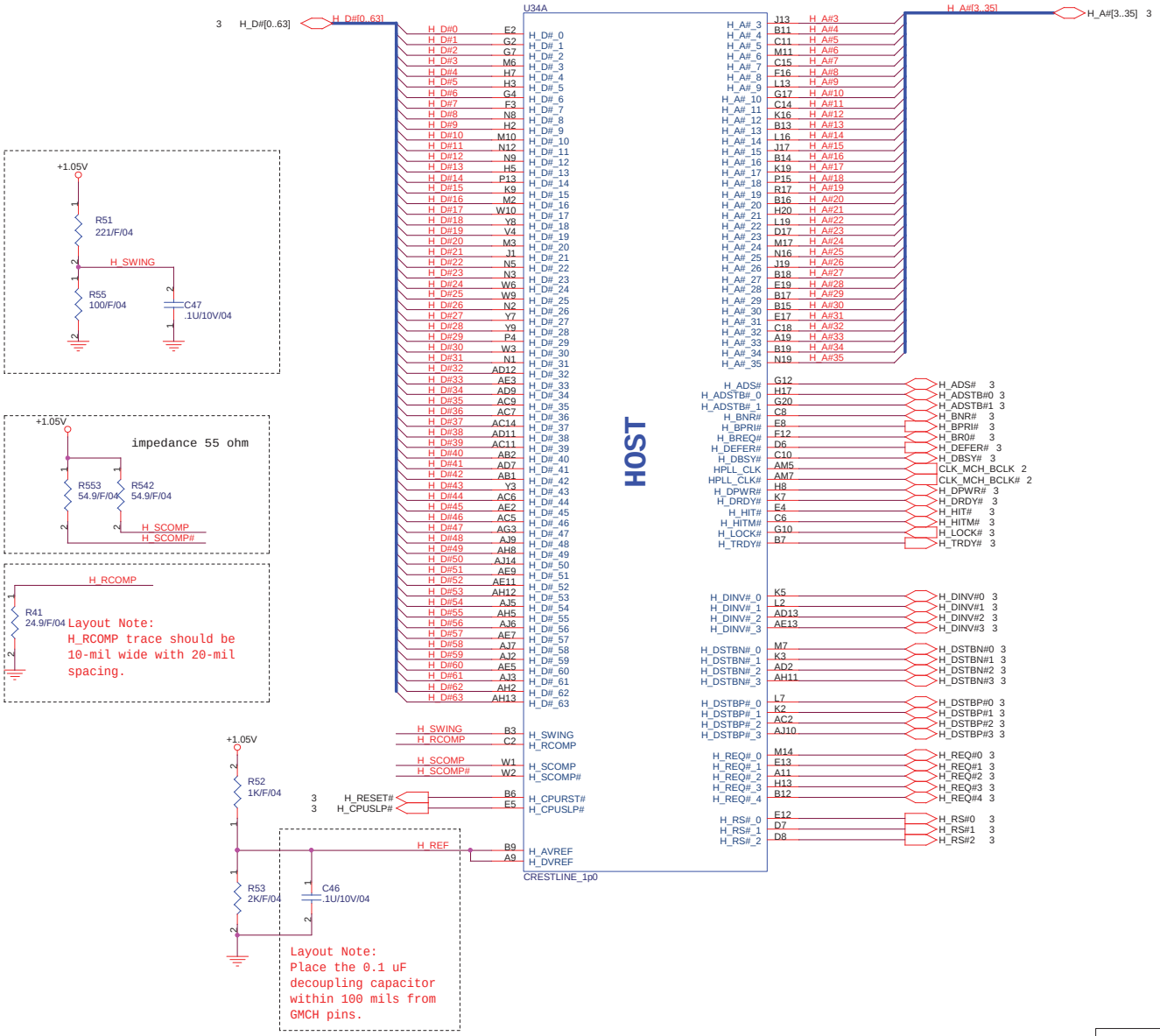
Size	Document Number	Rev
Custom	Merom Processor (POWER)	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 4 of 48

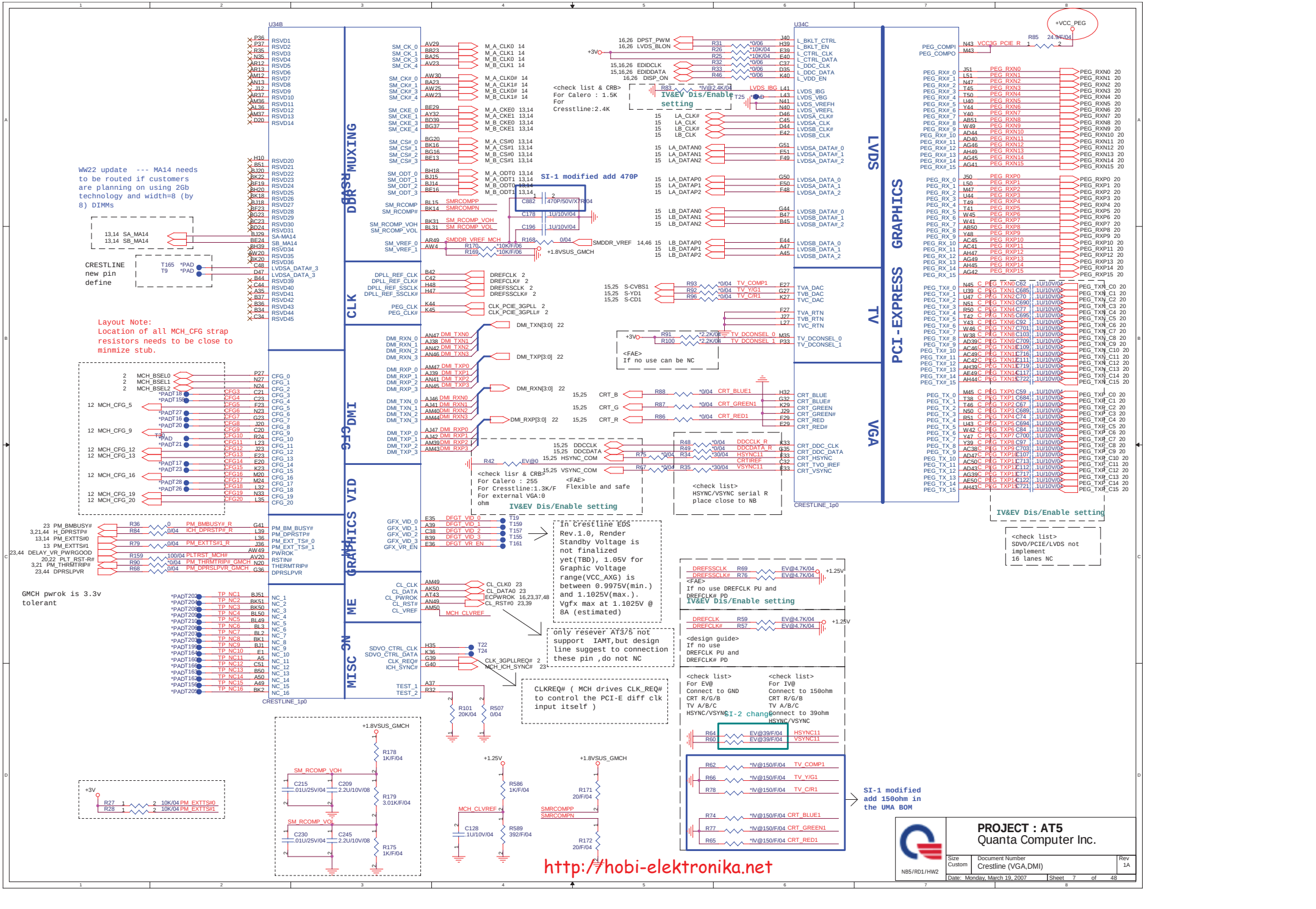


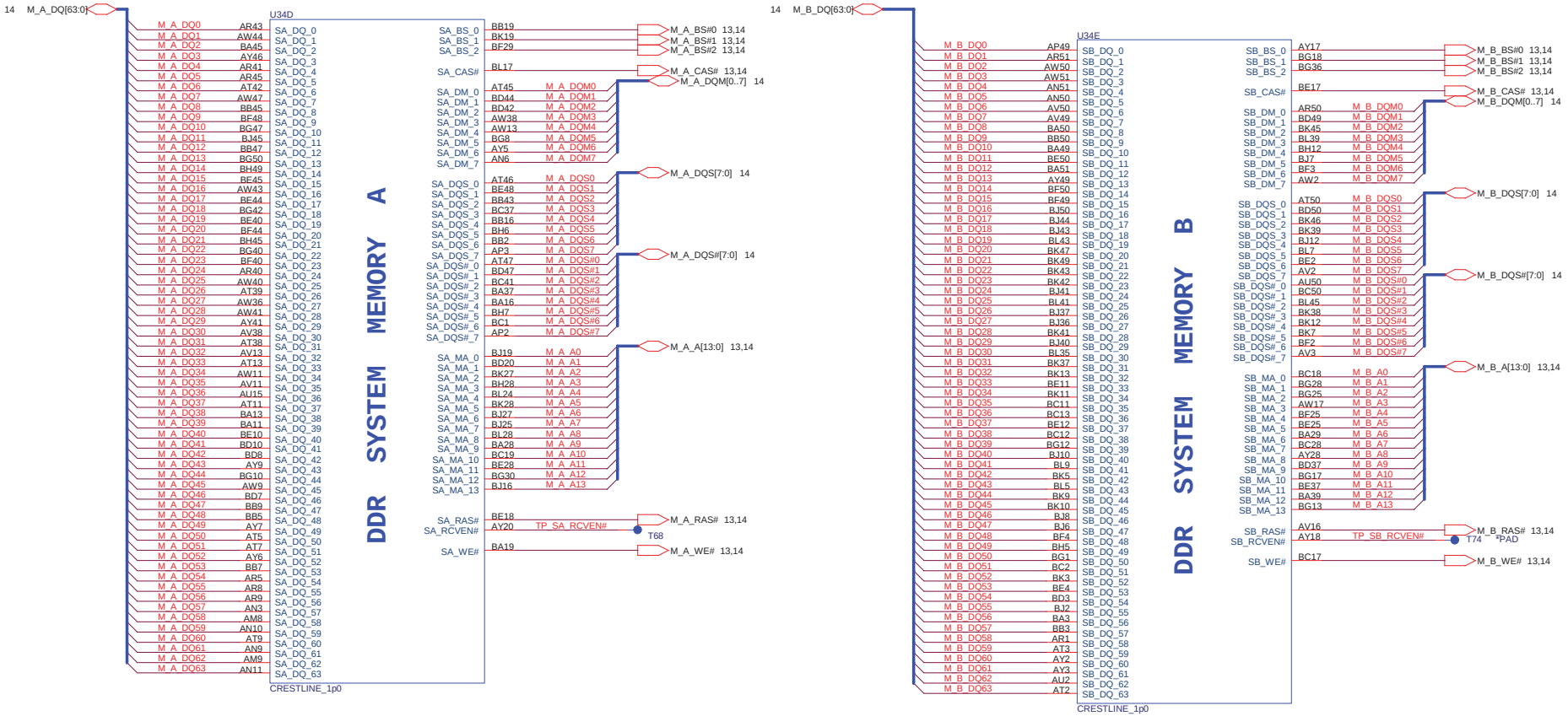
NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
	Size: B	Document Number: THERMAL LM86 — Rev: 1A
	Date: Monday, March 19, 2007	Sheet 5 of 48



http://hobi-elektronika.net

NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: Crestline (HOST)	Rev: 1A
Date: Monday, March 19, 2007	Sheet 6 of 48	


U34B
U34C
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
NC
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
WW22 update --- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs
CRESTLINE new pin define
Layout Note: Location of all MCH_CFG strap resistors needs to be close to minmize stub.
SI-1 modified add 470P
IV&EV Dis/Enable setting
GMCH pwrok is 3.3v tolerant
In crestline EDS Rev.1.0, Render Standby Voltage is not finalized yet(TBD), 1.05V for Graphic Voltage range(VCC_AXG) is between 0.9975V(min.) and 1.1025V(max.). Vgfx max at 1.1025V @ 8A (estimated)
only resever AT3/5 not support IAMT,but design line suggest to connection these pin ,do not NC
CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)
SI-2 change
SI-1 modified add 150ohm in the UMA BOM
CRESTLINE_1p0
PROJECT : AT5
Quanta Computer Inc.
Crestline (VGA,DMI)
Monday, March 19, 2007
http://hobi-elektronika.net

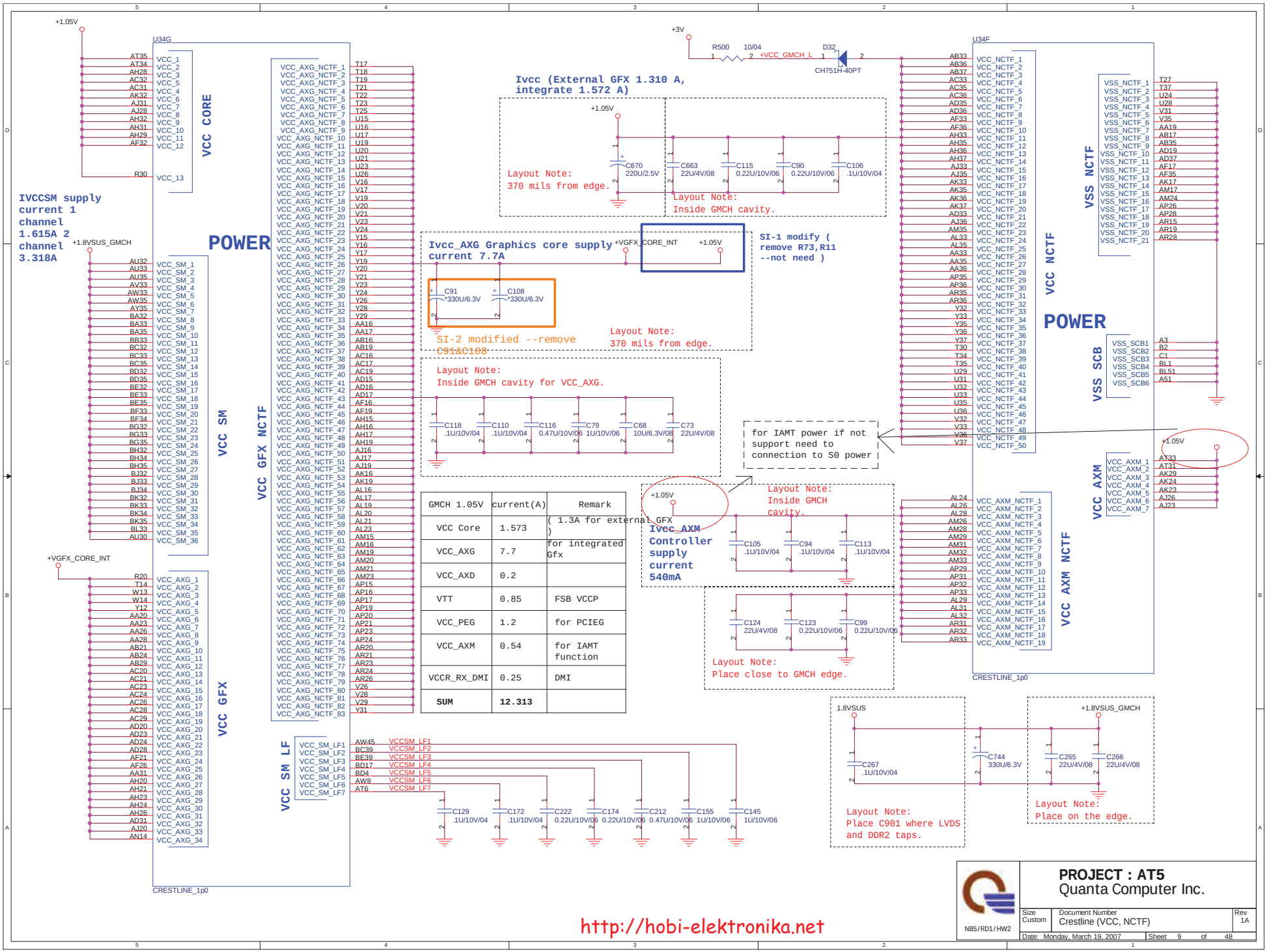


NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	1A

Date: Monday, March 19, 2007 Sheet 8 of 48



GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external GFX)
VCC_AXG	7.7	for integrated Gfx
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VCC, NCTF)	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 | Sheet 9 of 48

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

SI-1 modify
(NET name
wrong)

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

10uH+-20%_100mA

0.1Caps should be
placed 200 mils
with in its pins.

Ivcca_PEG_BG
supply current
100mA

Ivcc_VTT FSB
supply
current
0.85A

Place on the edge.

Reserved L81 pad for
inductor.

Place caps close
to VCC_AXD.

Ivcc_DMI supply
current 100mA

Place caps close
to VCC_AXF

+3V_VCC_HV

40 mil
wide

1uH+-20%_300mA

Ivcc_PEG
supply current
1.2A

SI-1 modified change

Ivcc_RX_DMI
supply current
250mA

SI-2
modified
for WW44
request

SI-2 add for UMA to
fix TV-out noise

22nF & 0.1uF for
VCC_TVDACA:C_R should
be placed with in 250
mils from Crestline.

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

IV&EV Dis/Enable setting

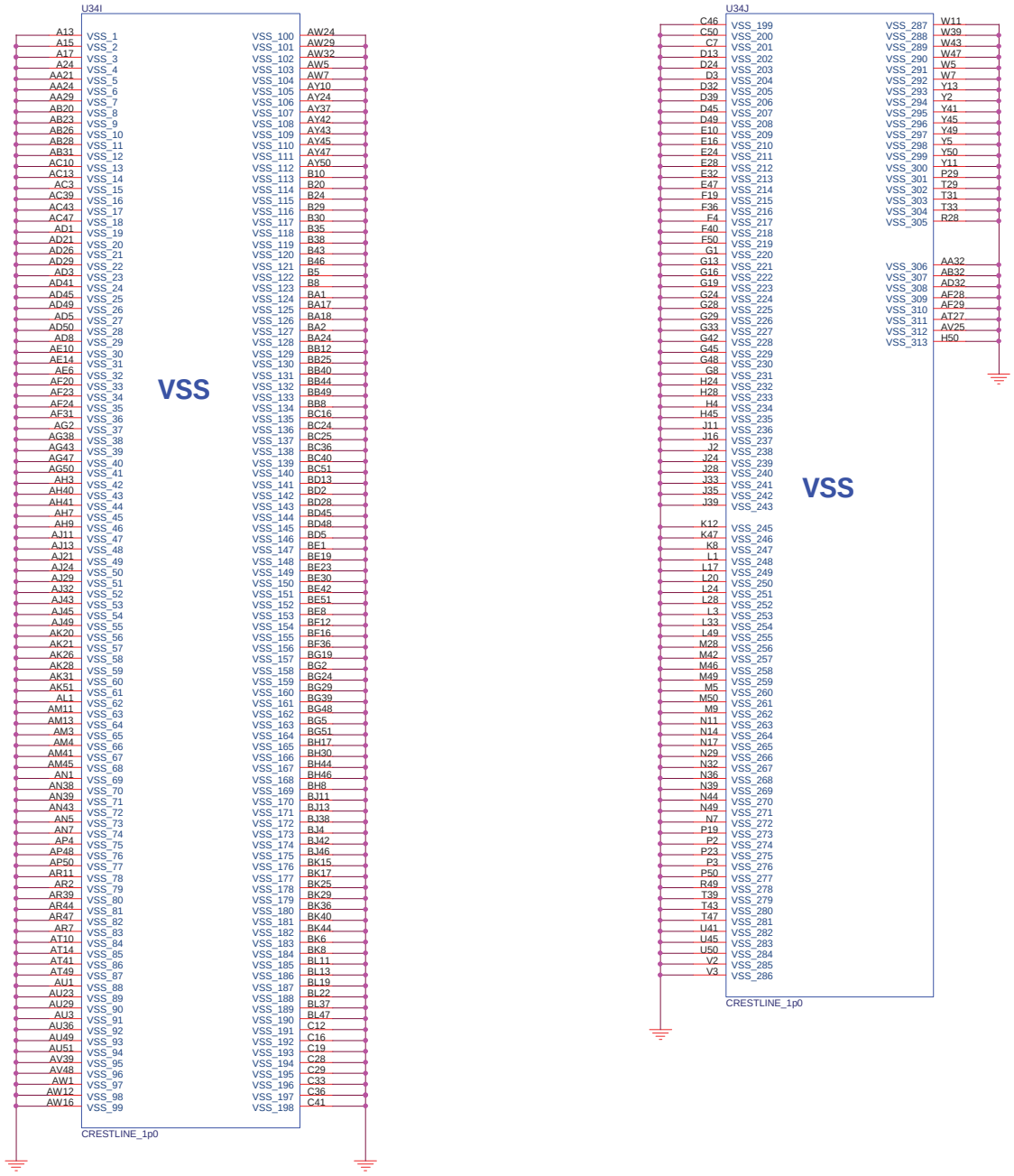
CRESTLINE_1p0

PROJECT : AT5
Quanta Computer Inc.

N85/RD1/HW2

Size: Custom | Document Number: Crestline (POWER) | Rev: 1A

Date: Monday, March 19, 2007 | Sheet 10 of 48



NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VSS)	1A

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Strap table

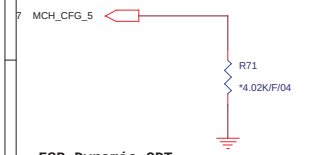
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

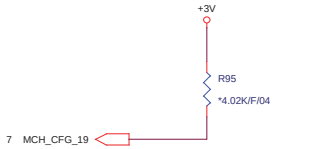
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

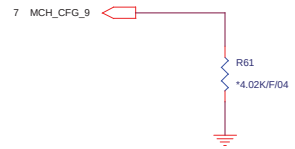


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

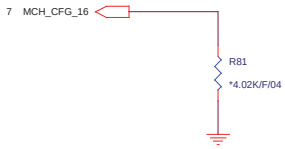


SDVO Present

Strap define at External DVI control page

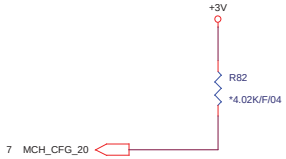
FSB Dynamic ODT

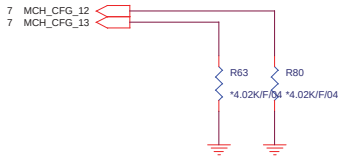
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

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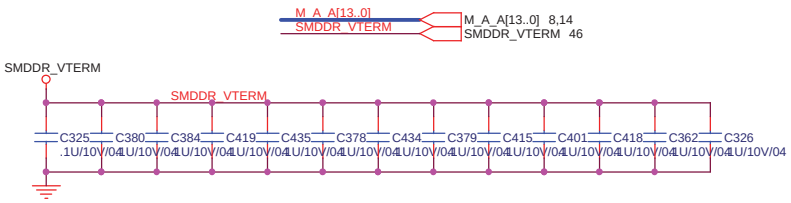
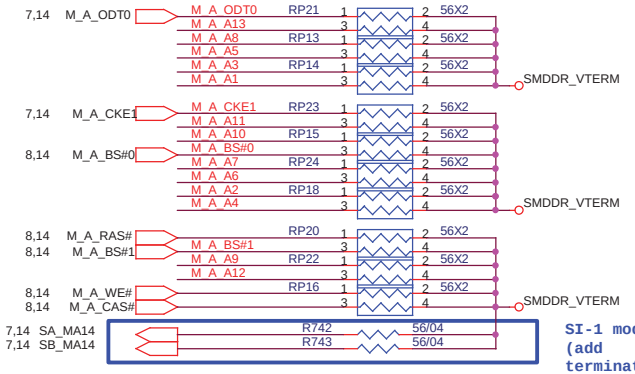
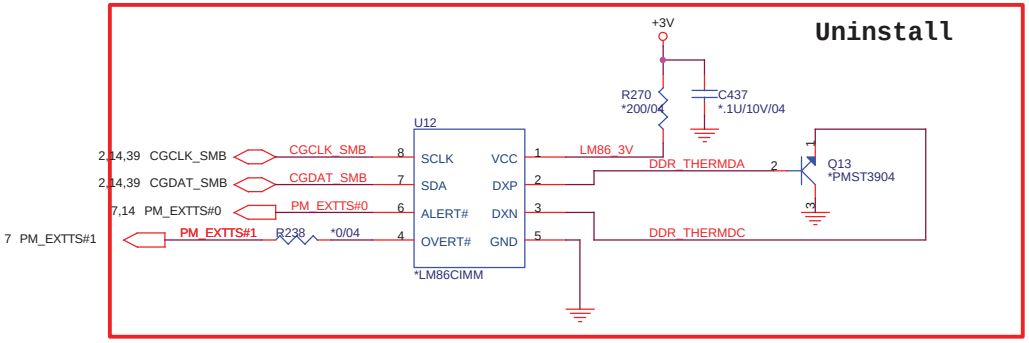
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

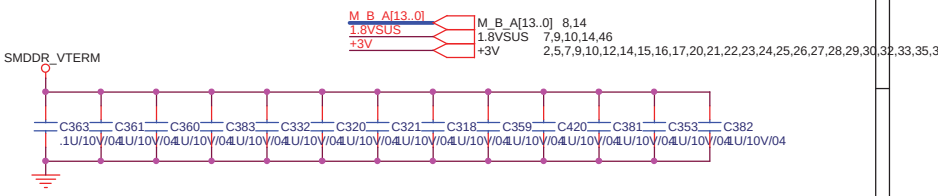




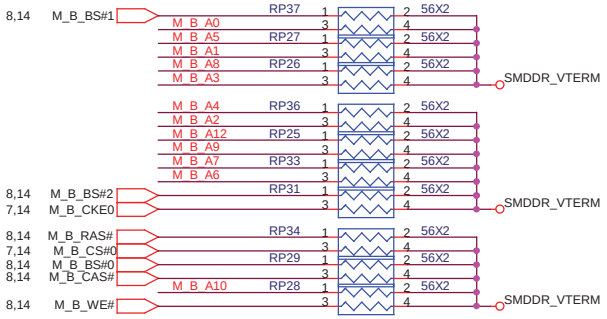
SI-1 modify (add terminater resistor)

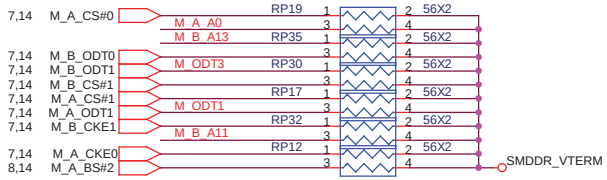


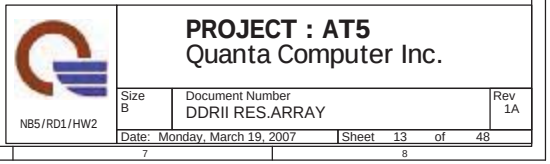
DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM







CGCLK_SMB
CGDAT_SMB

M_A_CKE[0..1]
M_A_CS#[0..1]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CLK0
M_A_CLK0#
M_A_CLK1
M_A_CLK1#
M_A_BS#[0..2]
M_A_ODT[0..1]
M_A_DQM[0..7]
M_A_DQ[0..63]
M_A_DQS[0..7]
M_A_A[13..0]

+3V
1.8VSUS

M_B_CKE[0..1]
M_B_CS#[0..1]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_BS#[0..2]
M_B_ODT[0..1]
M_B_DQM[0..7]
M_B_DQ[0..63]
M_B_DQS[0..7]
M_B_DQS#[0..7]
M_B_A[13..0]

PC2100 DDR2 SDRAM SO-DIMM (200P)

FOX=AS0A426-M2S-TR
CN26A

CKEA 0,1
H 9.2

FOX=AS0A426-MAS-TR
CN24A

CKEB 0,1
H 5.2

SMBus address A4

SMBus address A0

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM
SI-1 CHANGE
PM_EXTTS#0
SB_MA14
SA_MA14

FOX=AS0A426-M2S-TR
CN26B

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
SMDDR_VREF_DIMM
R226 0/06
SMDDR_VREF 7,46
R227
R603 *10K/F/06
*10K/F/06

Place these Caps near So-Dimm1.

1.8VSUS
C773 2.2U/6.3V/06
C775 2.2U/6.3V/06
C785 2.2U/6.3V/06
C444 2.2U/6.3V/06
C764 2.2U/6.3V/06
C770 .1U/10V/04
C788 .1U/10V/04
C439 .1U/10V/04
C433 .1U/10V/04
C769 .1U/10V/04
C767 .1U/10V/04
SMDDR_VREF_DIMM
C772 .1U/10V/04
C768 2.2U/6.3V/06
+3V
C317 2.2U/6.3V/06
C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

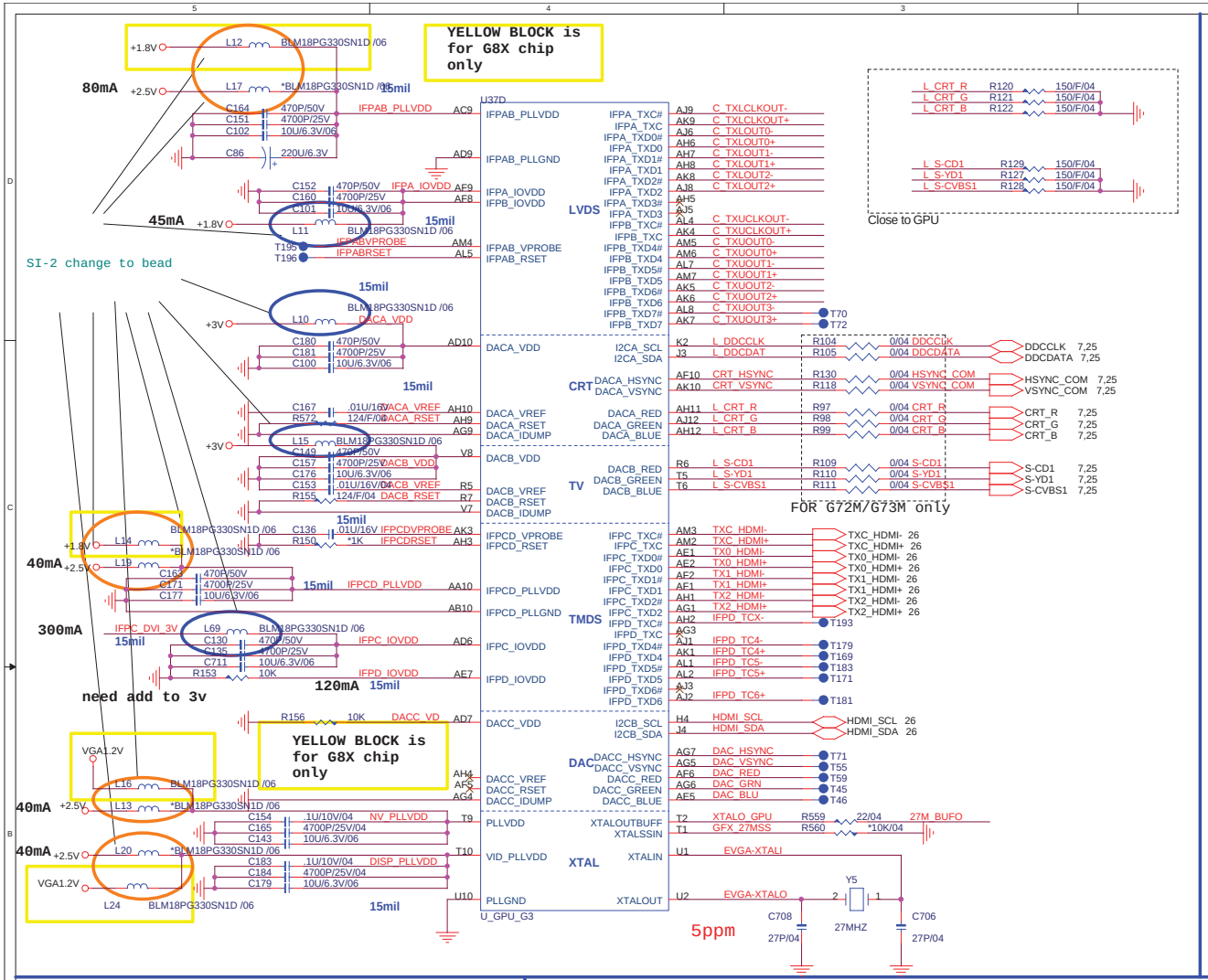
1.8VSUS
C774 2.2U/6.3V/06
C786 2.2U/6.3V/06
C784 2.2U/6.3V/06
C759 2.2U/6.3V/06
C760 .1U/10V/04
C776 .1U/10V/04
C789 .1U/10V/04
C787 .1U/10V/04
C443 .1U/10V/04
C765 .1U/10V/04
C766 .1U/10V/04
SMDDR_VREF_DIMM
C371 .1U/10V/04
C373 2.2U/6.3V/06
+3V
C372 2.2U/6.3V/06
C385 .1U/10V/04

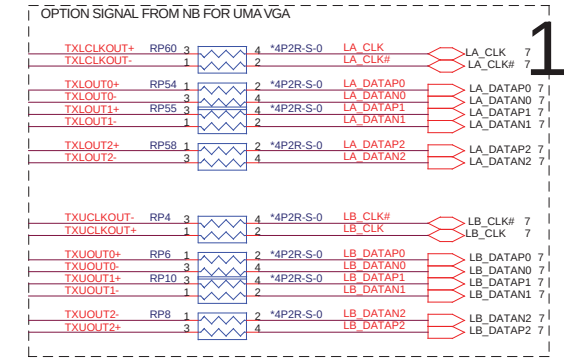
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.

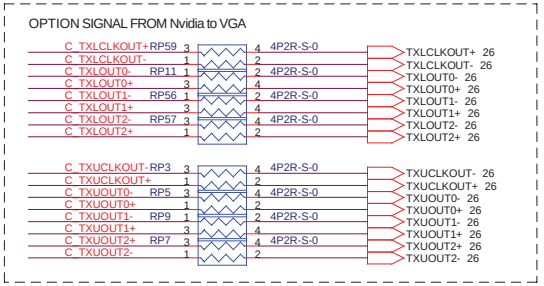
N8S/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

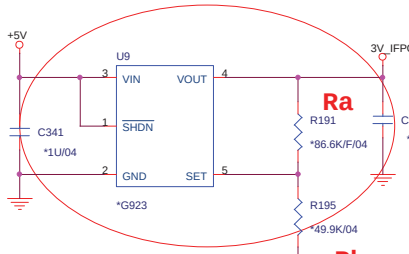
Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	1A
Date: Monday, March 19, 2007	Sheet 14 of 48	



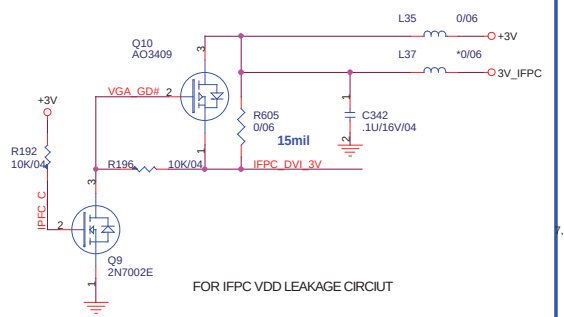


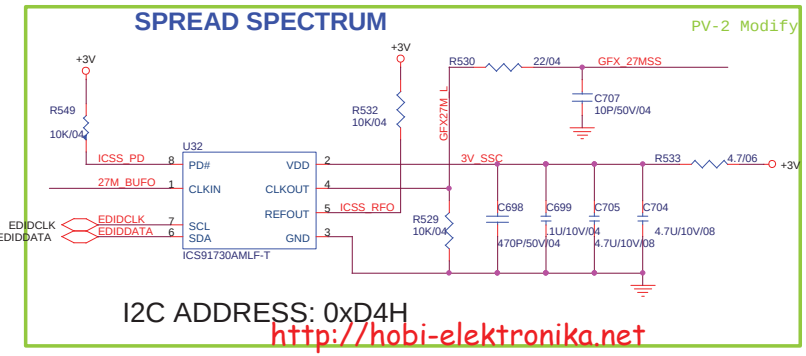


C34: PUN issue reserve
U54,C950,c949,R726,R727



Vout=1.25(1+Ra/Rb)

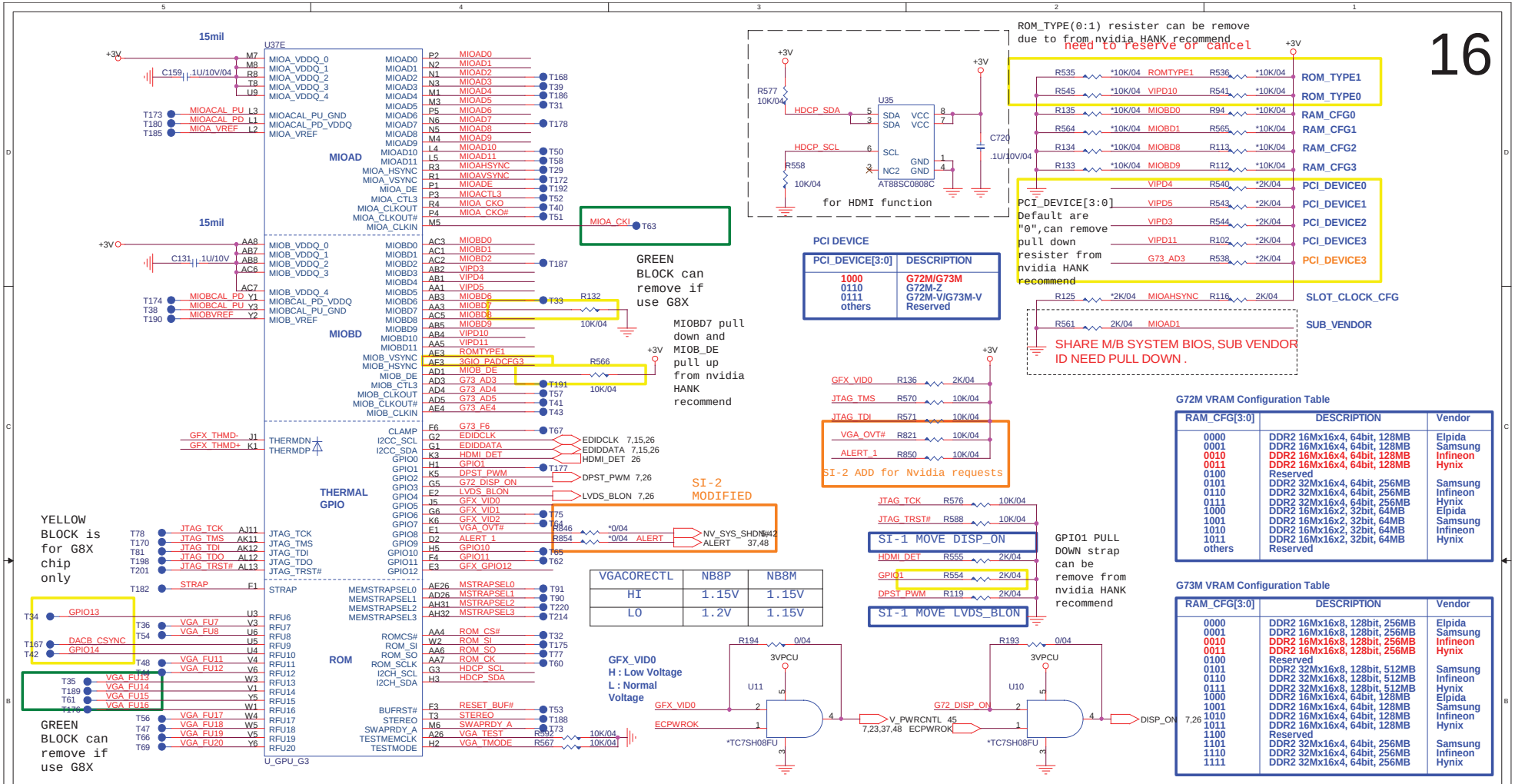




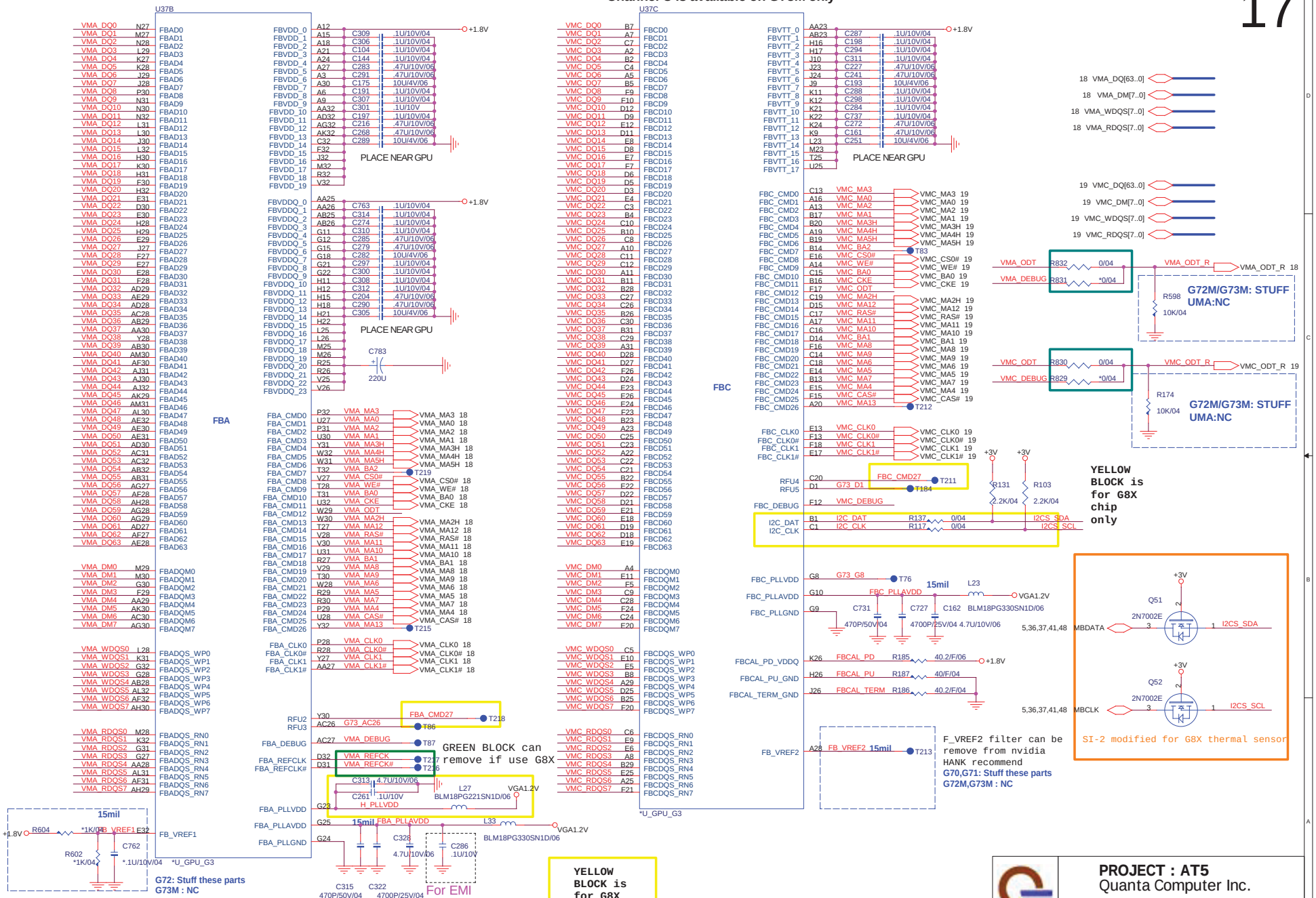
NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

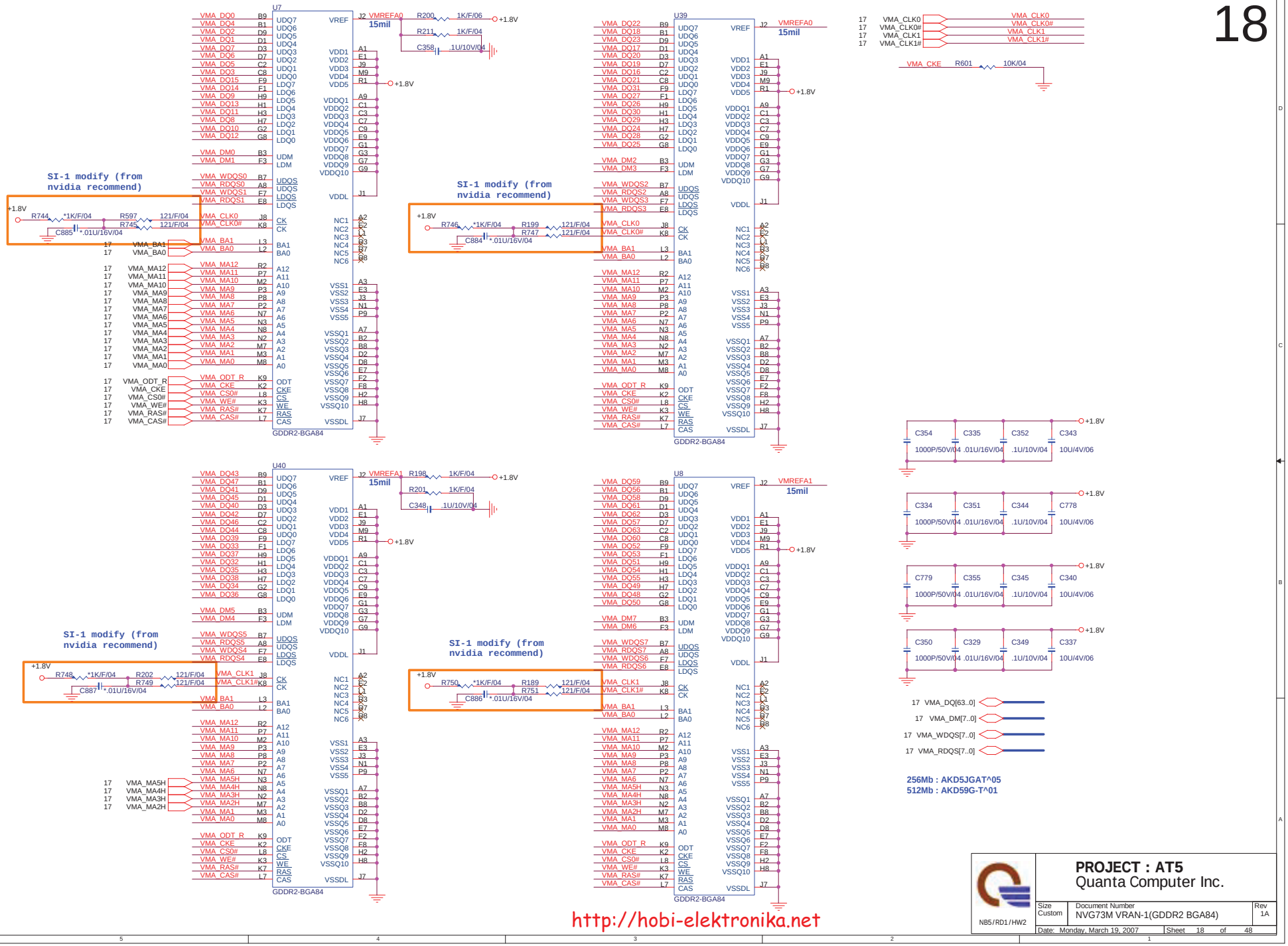
Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	1A
Date: Monday, March 19, 2007	Sheet 15 of 48	

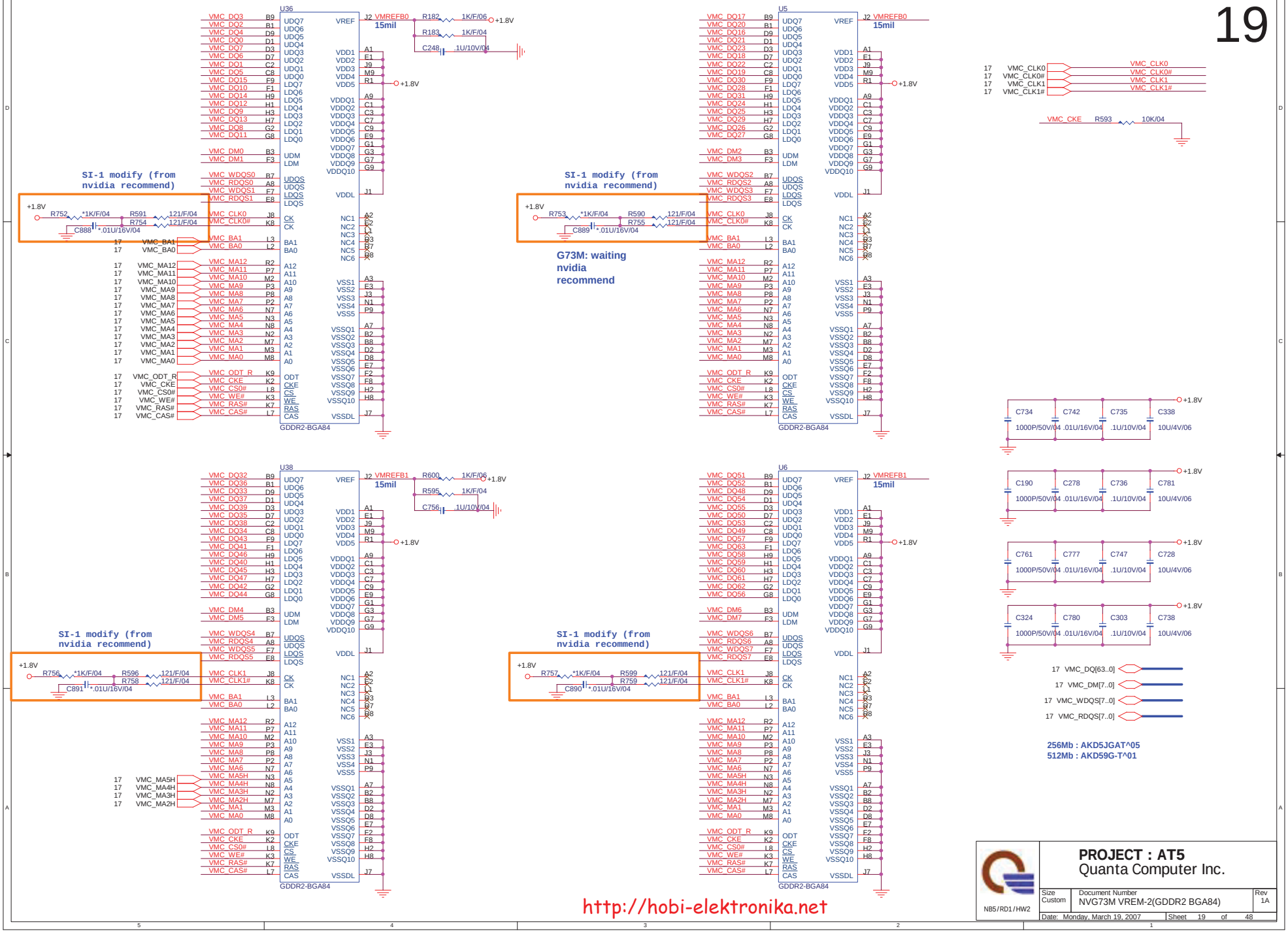

15mil
U37E
MIOAD
MIOBD
THERMAL GPIO
ROM
U_GPU_G3
ROM_TYPE(0:1) resister can be remove due to from nvidia HANK recommend
need to reserve or cancel
ROM_TYPE1
ROM_TYPE0
RAM_CFG0
RAM_CFG1
RAM_CFG2
RAM_CFG3
PCI_DEVICE0
PCI_DEVICE1
PCI_DEVICE2
PCI_DEVICE3
SLOT_CLOCK_CFG
SUB_VENDOR
PCI_DEVICE[3:0] Default are "0",can remove pull down resister from nvidia HANK recommend
for HDMI function
AT88SC0808C
PCI DEVICE
PCI_DEVICE[3:0] DESCRIPTION
1000 G72M/G73M
0110 G72M-Z
0111 G72M-V/G73M-V
others Reserved
GREEN BLOCK can remove if use G8X
MIOBD7 pull down and MIOB_DE pull up from nvidia HANK recommend
SHARE M/B SYSTEM BIOS, SUB VENDOR ID NEED PULL DOWN .
SI-2 MODIFIED
SI-2 ADD for Nvidia requests
SI-1 MOVE DISP_ON
SI-1 MOVE LVDS_BLON
GPIO1 PULL DOWN strap can be remove from nvidia HANK recommend
YELLOW BLOCK is for G8X chip only
GREEN BLOCK can remove if use G8X
VGACORECTL NB8P NB8M
HI 1.15V 1.15V
LO 1.2V 1.15V
GFX_VID0 H : Low Voltage L : Normal Voltage
G72M VRAM Configuration Table
RAM_CFG[3:0] DESCRIPTION Vendor
0000 DDR2 16Mx16x4, 64bit, 128MB Elpida
0001 DDR2 16Mx16x4, 64bit, 128MB Samsung
0010 DDR2 16Mx16x4, 64bit, 128MB Infineon
0011 DDR2 16Mx16x4, 64bit, 128MB Hynix
0100 Reserved
0101 DDR2 32Mx16x4, 64bit, 256MB Samsung
0110 DDR2 32Mx16x4, 64bit, 256MB Infineon
0111 DDR2 32Mx16x4, 64bit, 256MB Hynix
1000 DDR2 16Mx16x2, 32bit, 64MB Elpida
1001 DDR2 16Mx16x2, 32bit, 64MB Samsung
1010 DDR2 16Mx16x2, 32bit, 64MB Infineon
1011 DDR2 16Mx16x2, 32bit, 64MB Hynix
others Reserved
G73M VRAM Configuration Table
RAM_CFG[3:0] DESCRIPTION Vendor
0000 DDR2 16Mx16x8, 128bit, 256MB Elpida
0001 DDR2 16Mx16x8, 128bit, 256MB Samsung
0010 DDR2 16Mx16x8, 128bit, 256MB Infineon
0011 DDR2 16Mx16x8, 128bit, 256MB Hynix
0100 Reserved
0101 DDR2 32Mx16x8, 128bit, 512MB Samsung
0110 DDR2 32Mx16x8, 128bit, 512MB Infineon
0111 DDR2 32Mx16x8, 128bit, 512MB Hynix
1000 DDR2 16Mx16x4, 64bit, 128MB Elpida
1001 DDR2 16Mx16x4, 64bit, 128MB Samsung
1010 DDR2 16Mx16x4, 64bit, 128MB Infineon
1011 DDR2 16Mx16x4, 64bit, 128MB Hynix
1100 Reserved
1101 DDR2 32Mx16x4, 64bit, 256MB Samsung
1110 DDR2 32Mx16x4, 64bit, 256MB Infineon
1111 DDR2 32Mx16x4, 64bit, 256MB Hynix
GPIO12 G8X
HI AC MODE
LO BAT MODE
PV-2 MODIFIED
FOR BATTERY MODE throttling FUNCTION
VGA THERMAIL CIRCUIT
Default are "0",can remove pull down resister from nvidia HANK recommend
PEX_PLL_EN
3GIO_PADCFG_LUT_ADR0
3GIO_PADCFG_LUT_ADR1
3GIO_PADCFG_LUT_ADR2
3GIO_PADCFG_LUT_ADR3
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M (ROM/GPIO/STRAP)
Rev 1A
Date: Monday, March 19, 2007
Sheet 16 of 48

Channel C is available on G73M only



NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: NVG73M (MEM I/F)	Rev: 1A
Date: Monday, March 19, 2007	Sheet 17 of 48	


U7
U39
U40
U8
GDDR2-BGA84
SI-1 modify (from nvidia recommend)
SI-1 modify (from nvidia recommend)
SI-1 modify (from nvidia recommend)
SI-1 modify (from nvidia recommend)
VMREFA0
VMREFA1
15mil
+1.8V
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
VMA_CKE
R601 10K/04
C354 C335 C352 C343
C334 C351 C344 C778
C779 C355 C345 C340
C350 C329 C349 C337
1000P/50V/04 .01U/16V/04 .1U/10V/04 10U/4V/06
17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M VRAN-1(GDDR2 BGA84)
Rev 1A
Date: Monday, March 19, 2007
Sheet 18 of 48


U36
SI-1 modify (from nvidia recommend)
R752 *1K/F/04
R591 121/F/04
R754 121/F/04
C888 *.01U/16V/04
VMC_CLK0
VMC_CLK0#
VMC_BA1
VMC_BA0
VMC_MA12
VMC_MA11
VMC_MA10
VMC_MA9
VMC_MA8
VMC_MA7
VMC_MA6
VMC_MA5
VMC_MA4
VMC_MA3
VMC_MA2
VMC_MA1
VMC_MA0
VMC_ODT_R
VMC_CKE
VMC_CS0#
VMC_WE#
VMC_RAS#
VMC_CAS#
VMC_WDQS0
VMC_RDQS0
VMC_WDQS1
VMC_RDQS1
VMC_DM0
VMC_DM1
VMC_DQ0
VMC_DQ1
VMC_DQ2
VMC_DQ3
VMC_DQ4
VMC_DQ5
VMC_DQ6
VMC_DQ7
VMC_DQ8
VMC_DQ9
VMC_DQ10
VMC_DQ11
VMC_DQ12
VMC_DQ13
VMC_DQ14
VMC_DQ15
VREF
J2 VMREFB0
15mil
R182 1K/F/06
R183 1K/F/04
C248 .1U/10V/04
+1.8V
GDDR2-BGA84
U5
SI-1 modify (from nvidia recommend)
R753 *1K/F/04
R590 121/F/04
R755 121/F/04
C889 *.01U/16V/04
G73M: waiting nvidia recommend
VMC_DQ17
VMC_DQ20
VMC_DQ16
VMC_DQ21
VMC_DQ23
VMC_DQ18
VMC_DQ22
VMC_DQ19
VMC_DQ30
VMC_DQ28
VMC_DQ31
VMC_DQ24
VMC_DQ25
VMC_DQ29
VMC_DQ26
VMC_DQ27
VMC_DM2
VMC_DM3
VMC_WDQS2
VMC_RDQS2
VMC_WDQS3
VMC_RDQS3
17 VMC_CLK0
17 VMC_CLK0#
17 VMC_CLK1
17 VMC_CLK1#
VMC_CKE R593 10K/04
C734 1000P/50V/04
C742 .01U/16V/04
C735 .1U/10V/04
C338 10U/4V/06
C190 1000P/50V/04
C278 .01U/16V/04
C736 .1U/10V/04
C781 10U/4V/06
C761 1000P/50V/04
C777 .01U/16V/04
C747 .1U/10V/04
C728 10U/4V/06
C324 1000P/50V/04
C780 .01U/16V/04
C303 .1U/10V/04
C738 10U/4V/06
17 VMC_DQ[63..0]
17 VMC_DM[7..0]
17 VMC_WDQS[7..0]
17 VMC_RDQS[7..0]
256Mb : AKD5JGAT^05
512Mb : AKD59G-T^01
U38
SI-1 modify (from nvidia recommend)
R756 *1K/F/04
R596 121/F/04
R758 121/F/04
C891 *.01U/16V/04
VMC_MA5H
VMC_MA4H
VMC_MA3H
VMC_MA2H
U6
SI-1 modify (from nvidia recommend)
R757 *1K/F/04
R599 121/F/04
R759 121/F/04
C890 *.01U/16V/04
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M VREM-2(GDDR2 BGA84)
Rev 1A
Date: Monday, March 19, 2007
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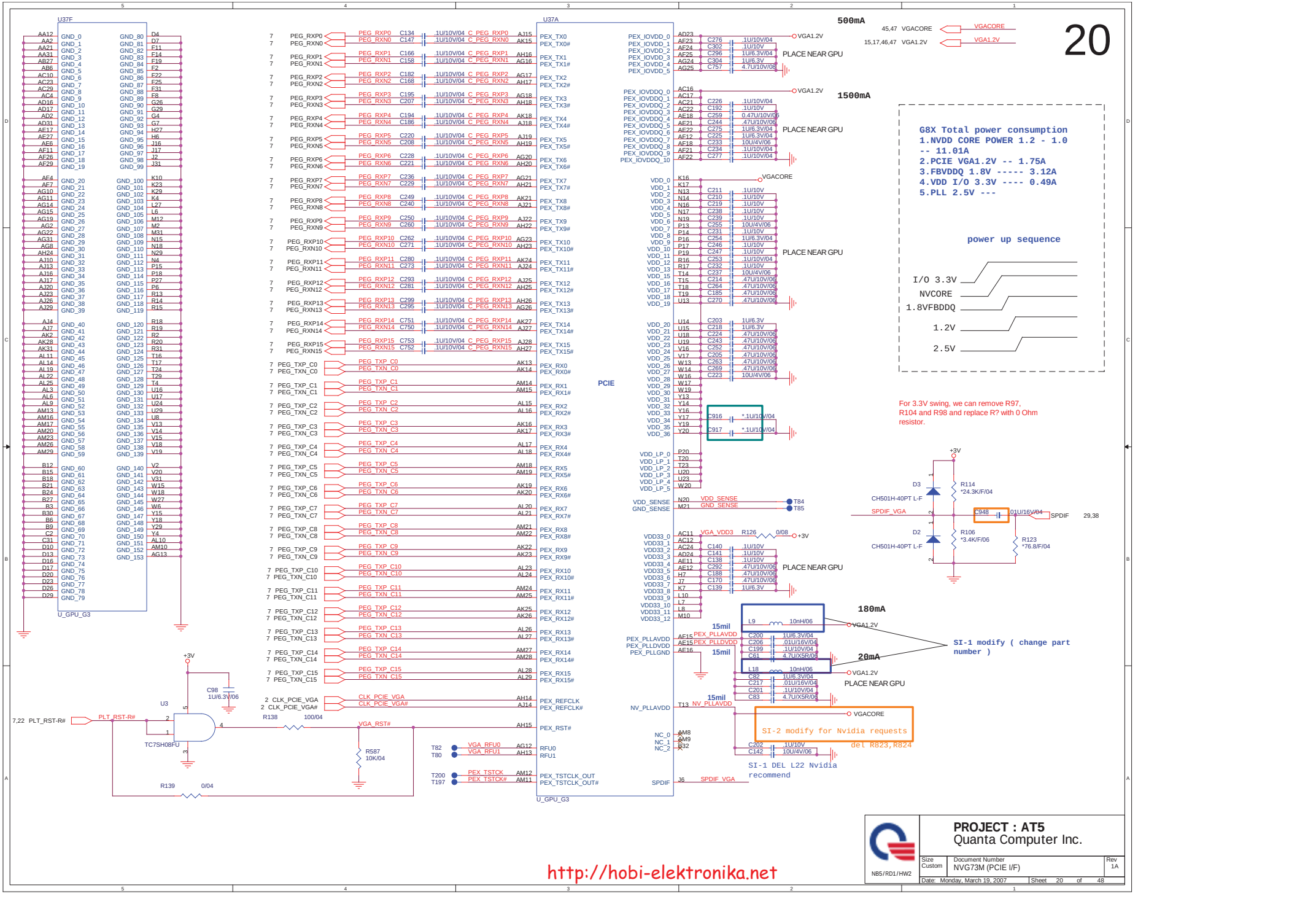
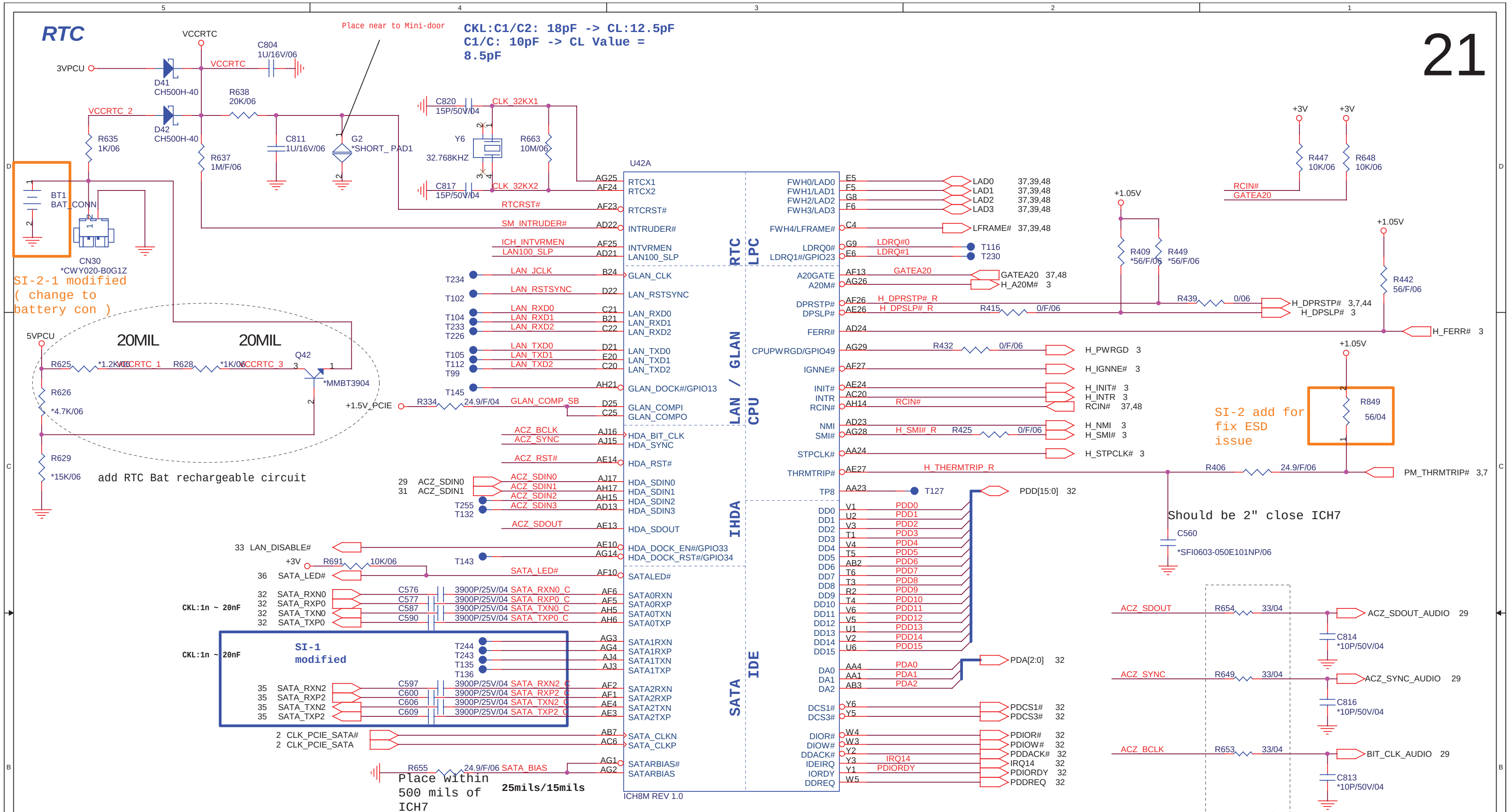

20
U37F
U37A
U_GPU_G3
PCIE
500mA
1500mA
180mA
20mA
PLACE NEAR GPU
VGA1.2V
VGACORE
G8X Total power consumption
1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
2.PCIE VGA1.2V -- 1.75A
3.FBVDDQ 1.8V ----- 3.12A
4.VDD I/O 3.3V ---- 0.49A
5.PLL 2.5V ---
power up sequence
I/O 3.3V
NVCORE
1.8VFBDDQ
1.2V
2.5V
For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.
SI-1 modify (change part number)
SI-2 modify for Nvidia requests
del R823,R824
SI-1 DEL L22 Nvidia recommend
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number NVG73M (PCIE I/F)
Rev 1A
Date: Monday, March 19, 2007
Sheet 20 of 48



RTC
VCCRTC
3VPCU
D41 CH500H-40
D42 CH500H-40
C804 1U/16V/06
VCCRTC_2
R638 20K/06
R635 1K/06
R637 1M/F/06
C811 1U/16V/06
G2 *SHORT_PAD1
Place near to Mini-door
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
C820 15P/50V/04
CLK_32KX1
Y6 32.768KHZ
R663 10M/06
C817 15P/50V/04
CLK_32KX2
BT1 BAT_CONN
CN30 *CWY020-B0G1Z
SI-2-1 modified (change to battery con)
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
LAN100_SLP
5VPCU
20MIL
20MIL
R625 *1.2K/06
R628 *1K/06
Q42 *MMBT3904
R626 *4.7K/06
R629 *15K/06
add RTC Bat rechargeable circuit
+1.5V_PCIE
R334 24.9/F/04
U42A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH8M REV 1.0
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0 … DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LAD0 37,39,48
LAD1 37,39,48
LAD2 37,39,48
LAD3 37,39,48
LFRAME# 37,39,48
T116
T230
GATEA20 37,48
H_A20M# 3
H_DPRSTP# 3,7,44
H_DPSLP# 3
H_FERR# 3
H_PWRGD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
RCIN# 37,48
H_NMI 3
H_SMI# 3
H_STPCLK# 3
PM_THRMTRIP# 3,7
T127
PDD[15:0] 32
PDA[2:0] 32
PDCS1# 32
PDCS3# 32
PDIOR# 32
PDIOW# 32
PDDACK# 32
IRQ14 32
PDIORDY 32
PDDREQ 32
+3V
R447 10K/06
R648 10K/06
RCIN#
GATEA20
+1.05V
R409 *56/F/06
R449 *56/F/06
R439 0/06
R415 0/F/06
R442 56/F/06
R432 0/F/06
R425 0/F/06
R849 56/04
SI-2 add for fix ESD issue
R406 24.9/F/06
Should be 2" close ICH7
C560 *SFI0603-050E101NP/06
33 LAN_DISABLE#
R691 10K/06
36 SATA_LED#
CKL:1n ~ 20nF
32 SATA_RXN0
32 SATA_RXP0
32 SATA_TXN0
32 SATA_TXP0
C576 C577 C587 C590 3900P/25V/04
SI-1 modified
35 SATA_RXN2
35 SATA_RXP2
35 SATA_TXN2
35 SATA_TXP2
C597 C600 C606 C609 3900P/25V/04
2 CLK_PCIE_SATA#
2 CLK_PCIE_SATA
R655 24.9/F/06 SATA_BIAS
Place within 500 mils of ICH7
25mils/15mils
29 ACZ_SDIN0
31 ACZ_SDIN1
ACZ_SDOUT
R654 33/04
ACZ_SDOUT_AUDIO 29
C814 *10P/50V/04
ACZ_SYNC
R649 33/04
ACZ_SYNC_AUDIO 29
C816 *10P/50V/04
ACZ_BCLK
R653 33/04
BIT_CLK_AUDIO 29
C813 *10P/50V/04
ACZ_RST#
R646 33/04
ACZ_RST#_AUDIO 29
intel check list define to stuff 33ohm
R639 33/04
ACZ_SDOUT_AUDIO_MDC 31
C807 *10P/50V/04
R640 33/04
ACZ_SYNC_AUDIO_MDC 31
C809 *10P/50V/04
R643 33/04
BIT_CLK_AUDIO_MDC 31
C810 *10P/50V/04
R645 33/04
ACZ_RST#_AUDIO_MDC 31

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

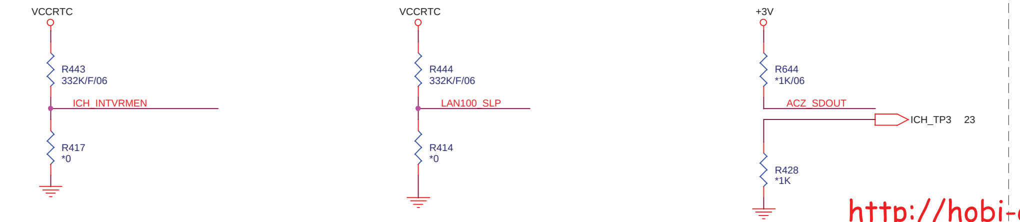
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



PROJECT : AT5
Quanta Computer Inc.

NB5/RD1/HW2

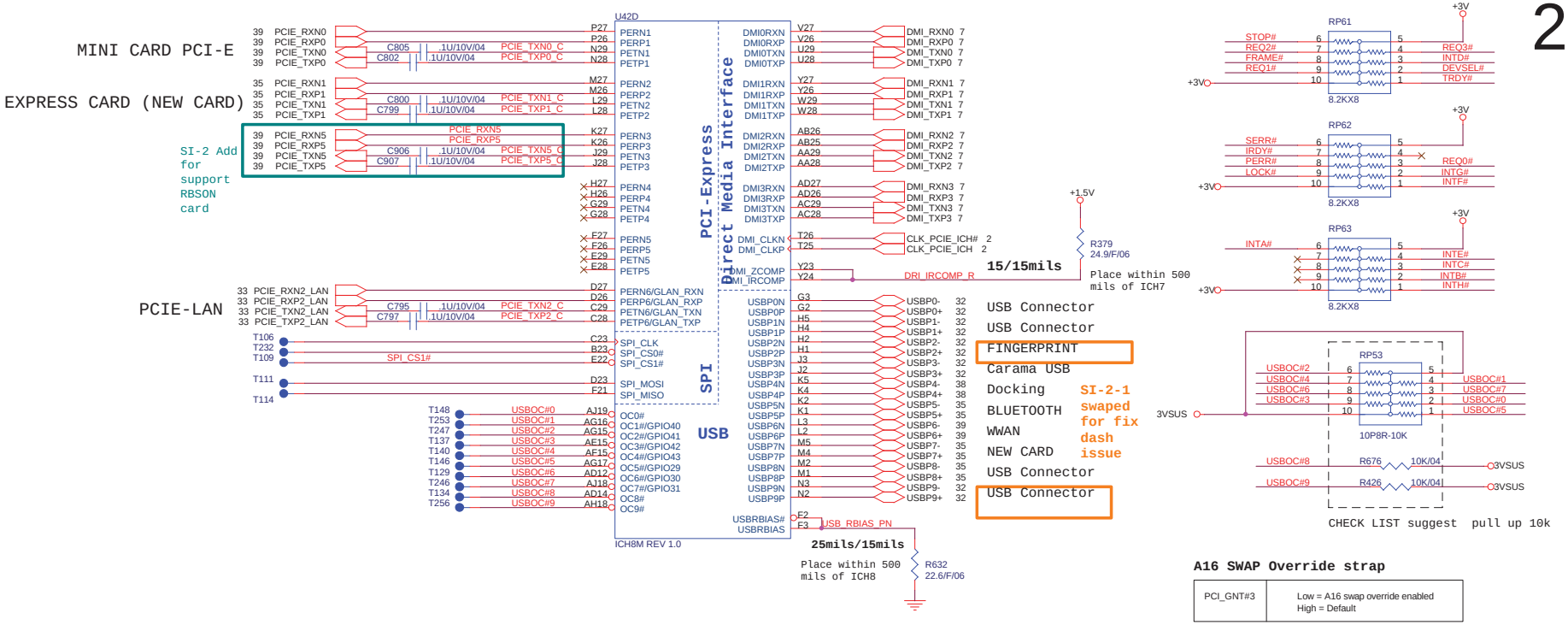
Size	Document Number	Rev
Custom	ICH7-M HOST(1/4)	1A

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

SI-2 Add for support RBSON card

PCIE-LAN



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

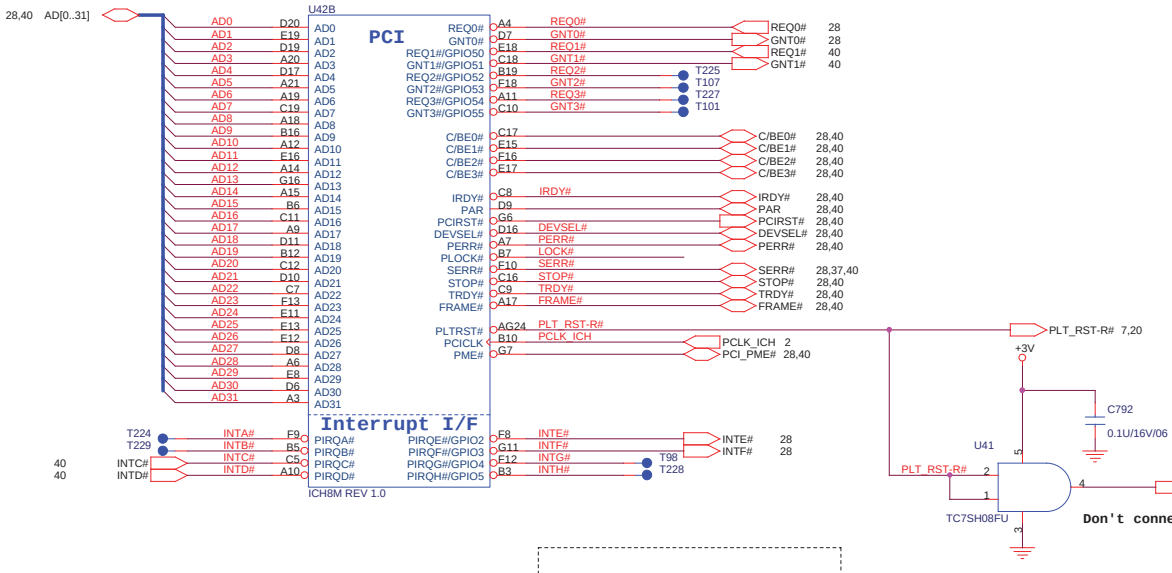
GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K



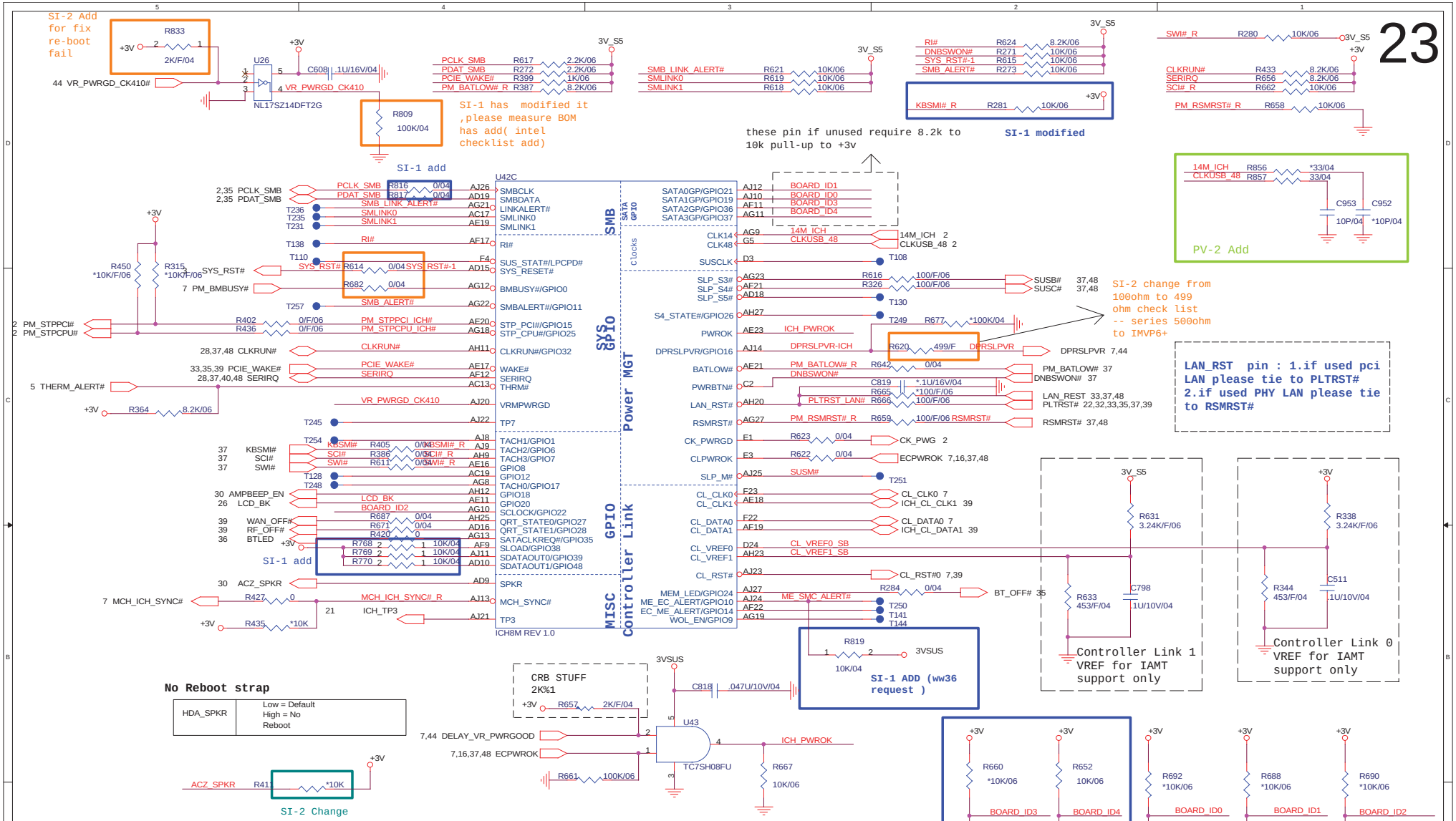
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PCLK_ICH R328 *0 C484 *33P/50V

for EMI request

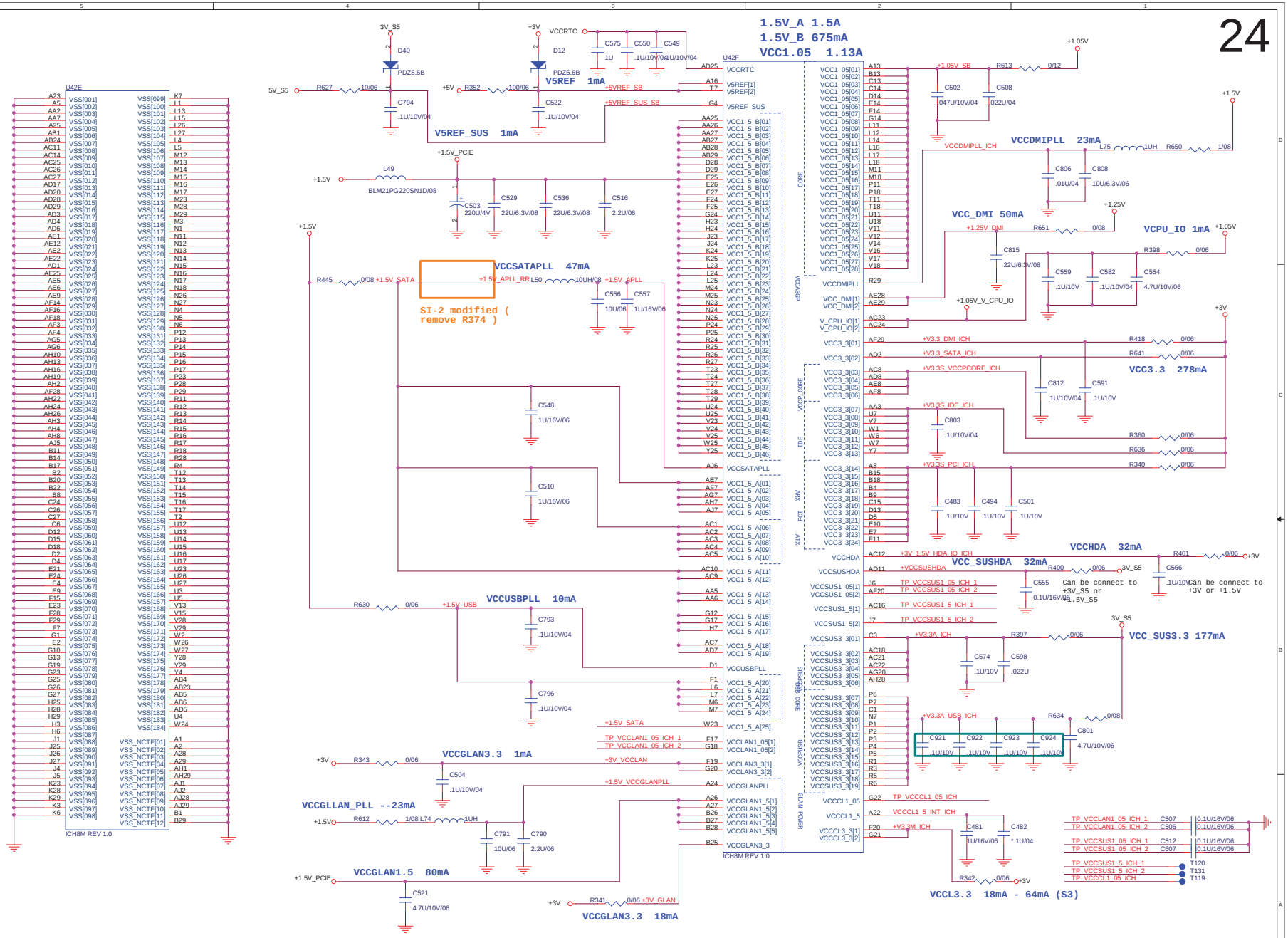
PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A
NB5/RD1/HW2	Date: Monday, March 19, 2007	Sheet 22 of 48

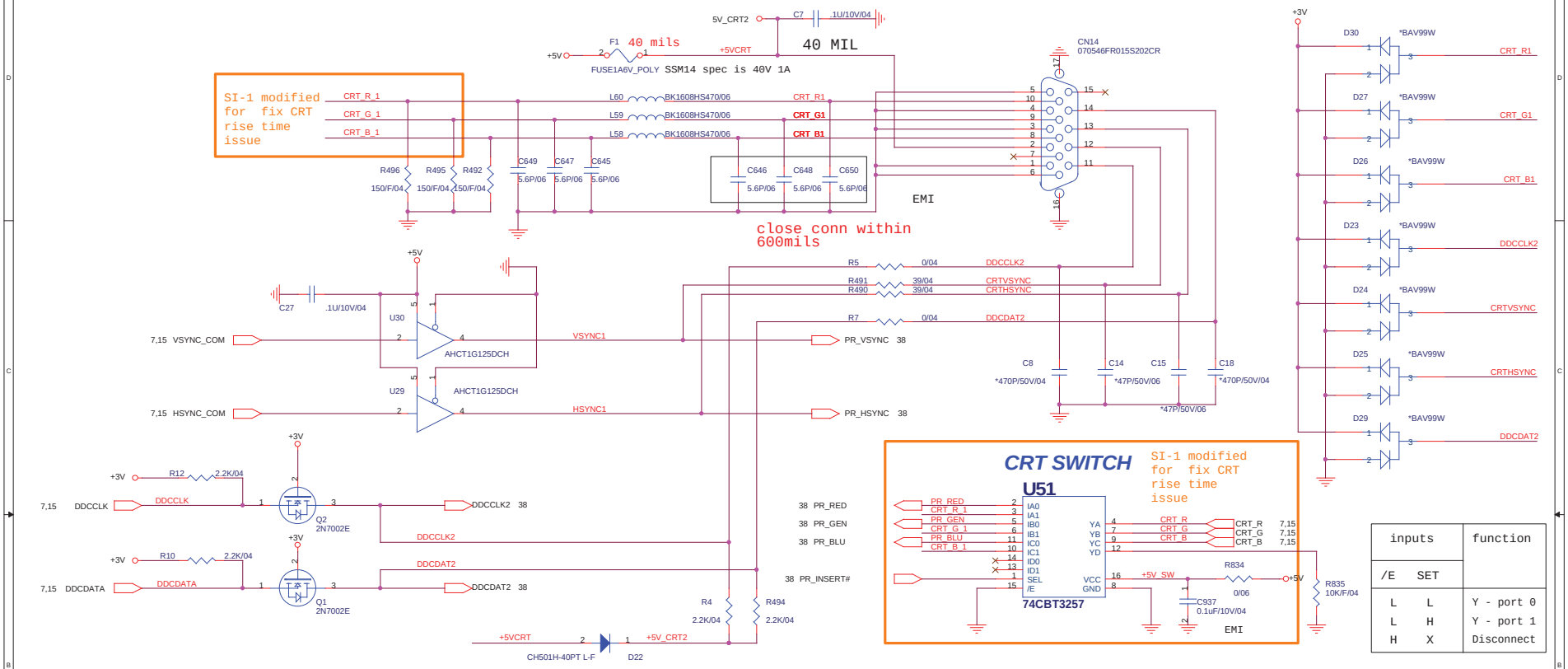


23

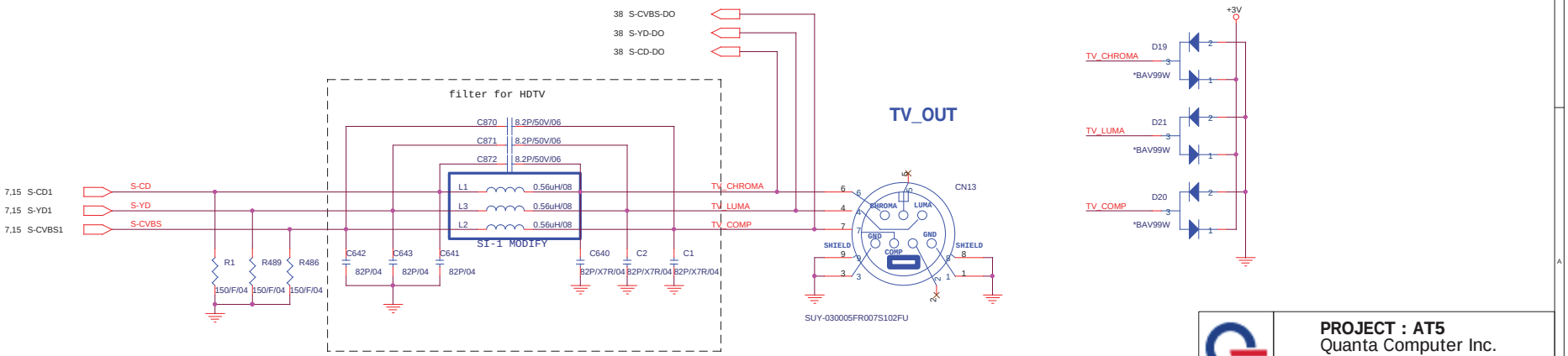
Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15″PAV Discrete 965PM+G86MV+128M (0:1:0)	17″ PAV Discrete 965PM+G86MV+128M (0:1:1)	17″ PAV Discrete 965PM+G84MV+256M (1:0:0)	17″ PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff


1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A
V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
SI-2 modified (remove R374)
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)
Can be connect to +3V_S5 or +1.5V_S5
Can be connect to +3V or +1.5V
ICH8M REV 1.0
http://hobi-elektronika.net
PROJECT : AT5
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number ICH7-M POWER(4/4)
Rev 1A
Date: Monday, March 19, 2007
Sheet 24 of 48

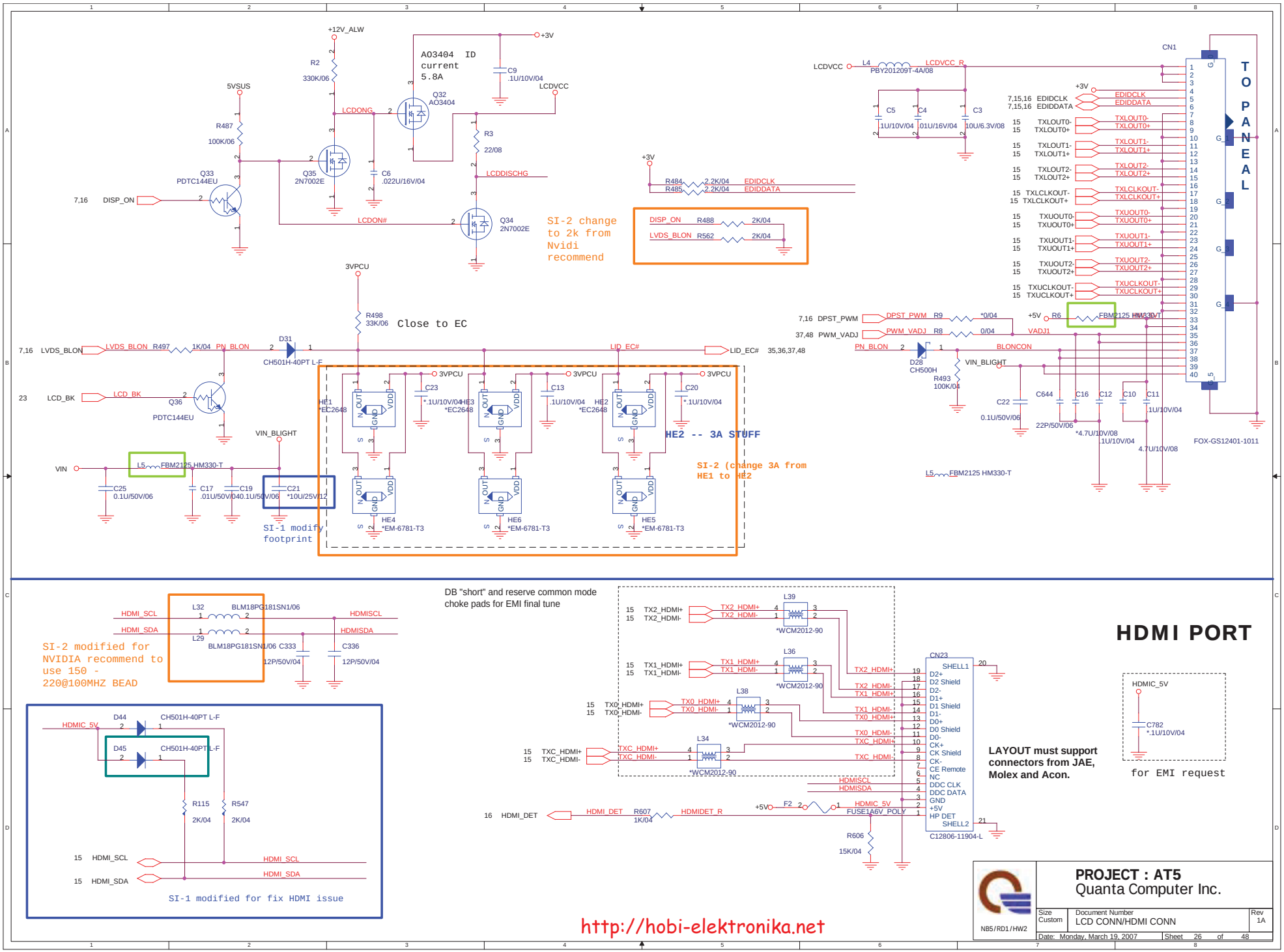
CRT PORT



inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect



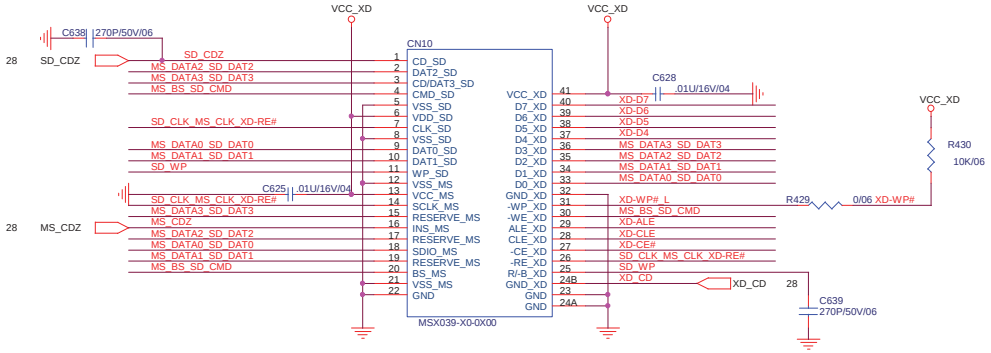
NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: CRT/TV_OUT	Rev: 1A
Date: Monday, March 19, 2007	Sheet 25 of 48	



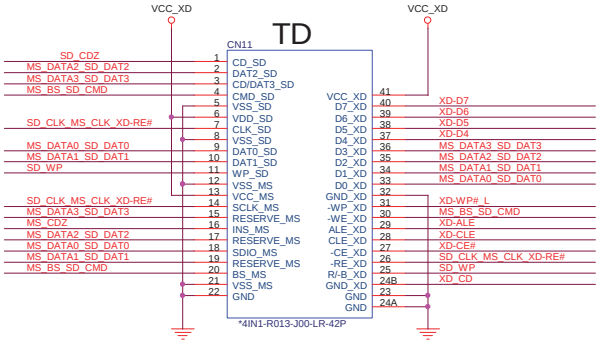
HDMI PORT

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN/HDMI CONN	Rev: 1A
Date: Monday, March 19, 2007	Sheet 26 of 48	

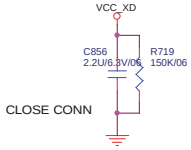
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

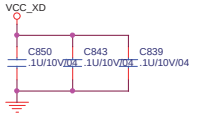


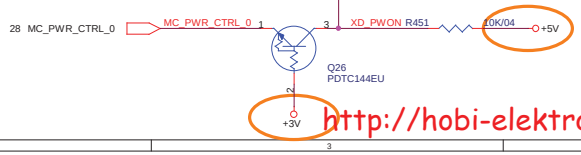
TD

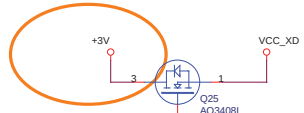


bom create 2'nd source

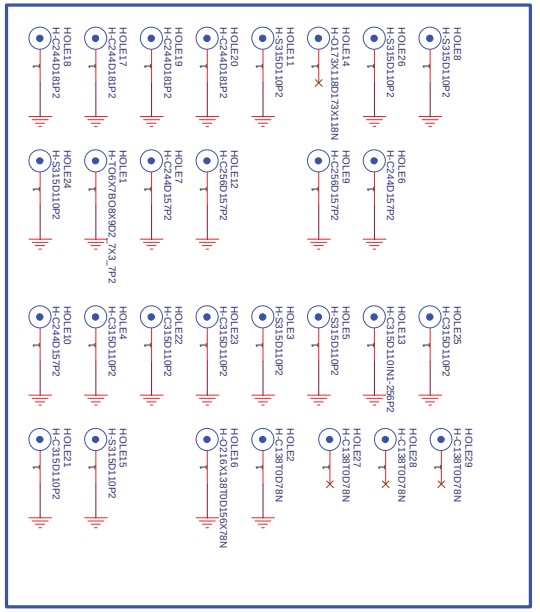




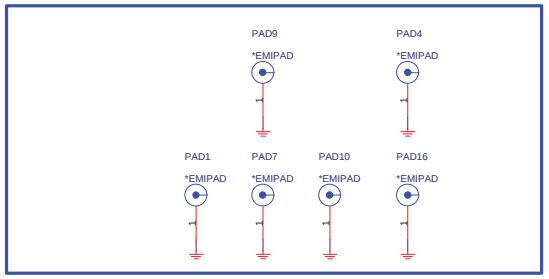




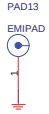
SCREW HOLE



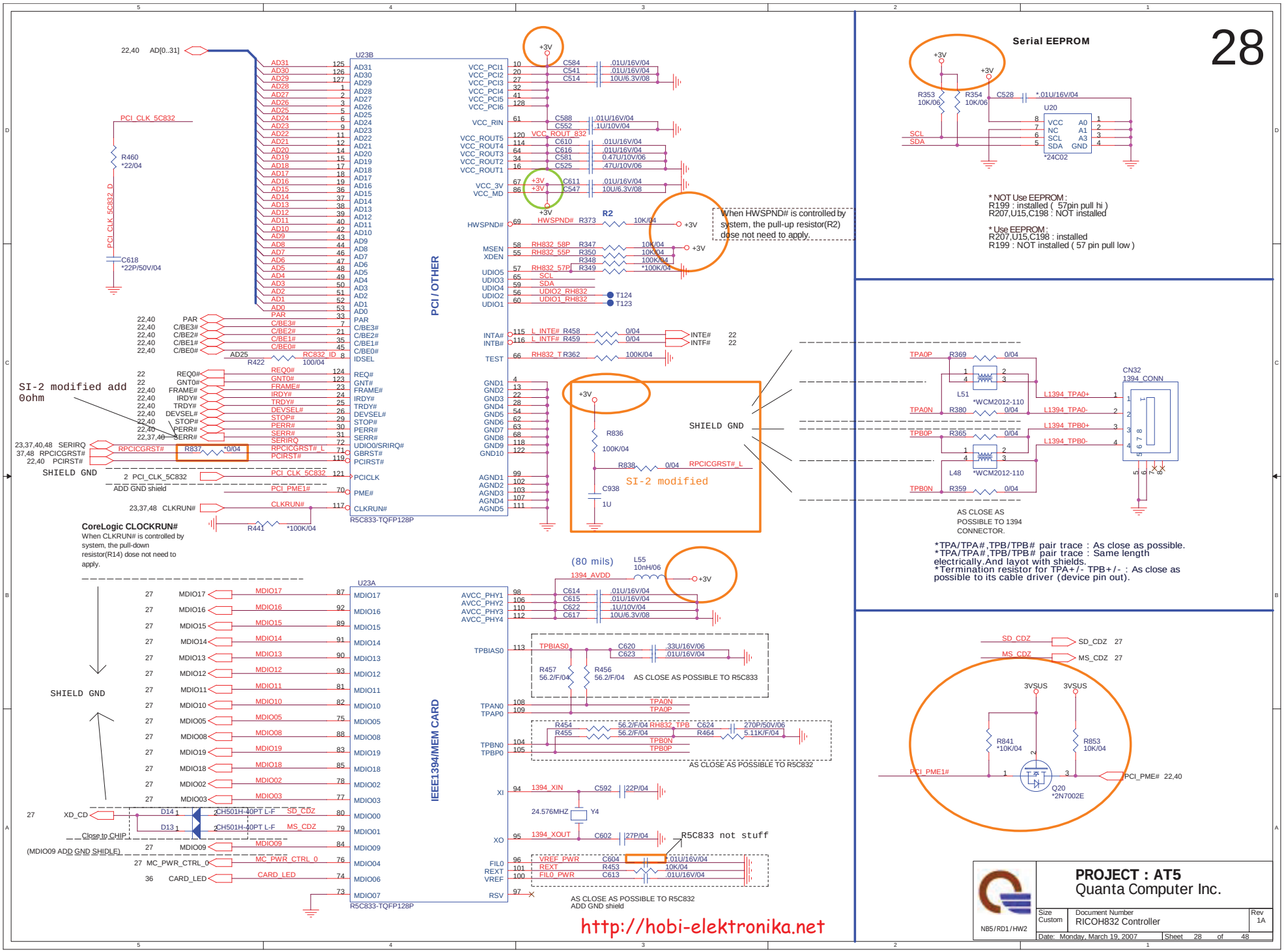
EMI PAD



moden cable sprig



NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: CARD READER/HOLE	Rev: 1A
Date: Monday, March 19, 2007	Sheet 27 of 48	



Serial EEPROM

* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed

* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)

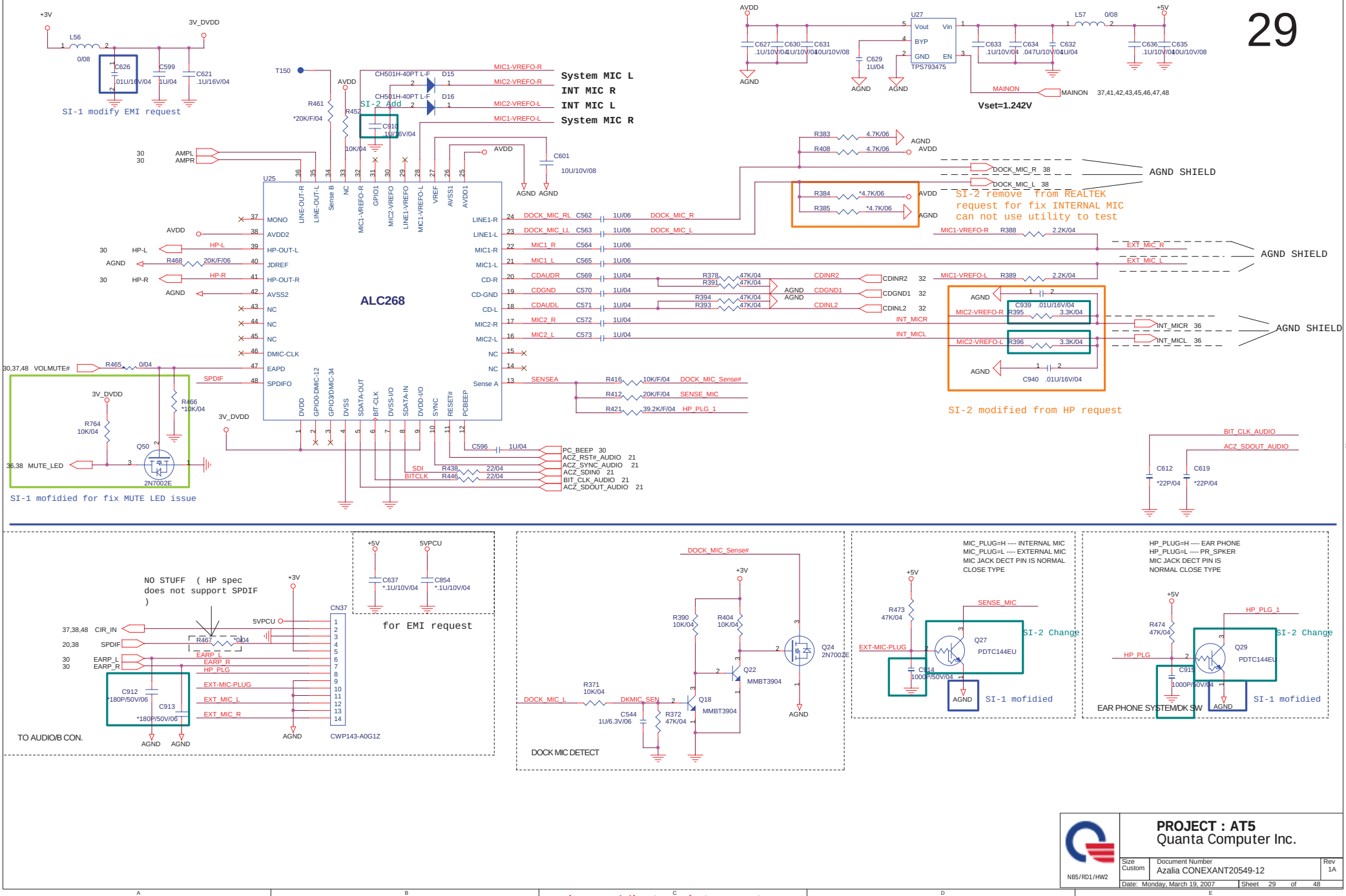
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layot with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RICOH832 Controller	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 28 of 48



AUDIO AMPLIFIER

INT. SPEAKER

PCSPK BEEP

LINE OUT Amplifier

SI-2 remove r739 ,r731 from realtek request for fix BO voice when audio jack unplug

0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB

PV-2 emi requests

SI-1 ADD EMI request

EMI requests change footprint

SI-1 DEL EMI request

SI-1 add R765 and remove * part

SI-1 add R807 and remove *part

TO CODE

TO AMP

LINE OUT Amplifier

MAX4411 EP can NOT be connected to GND. Please leave EP pins floating.

SI-2 modified from HP recommend

TPA0312 PWP24

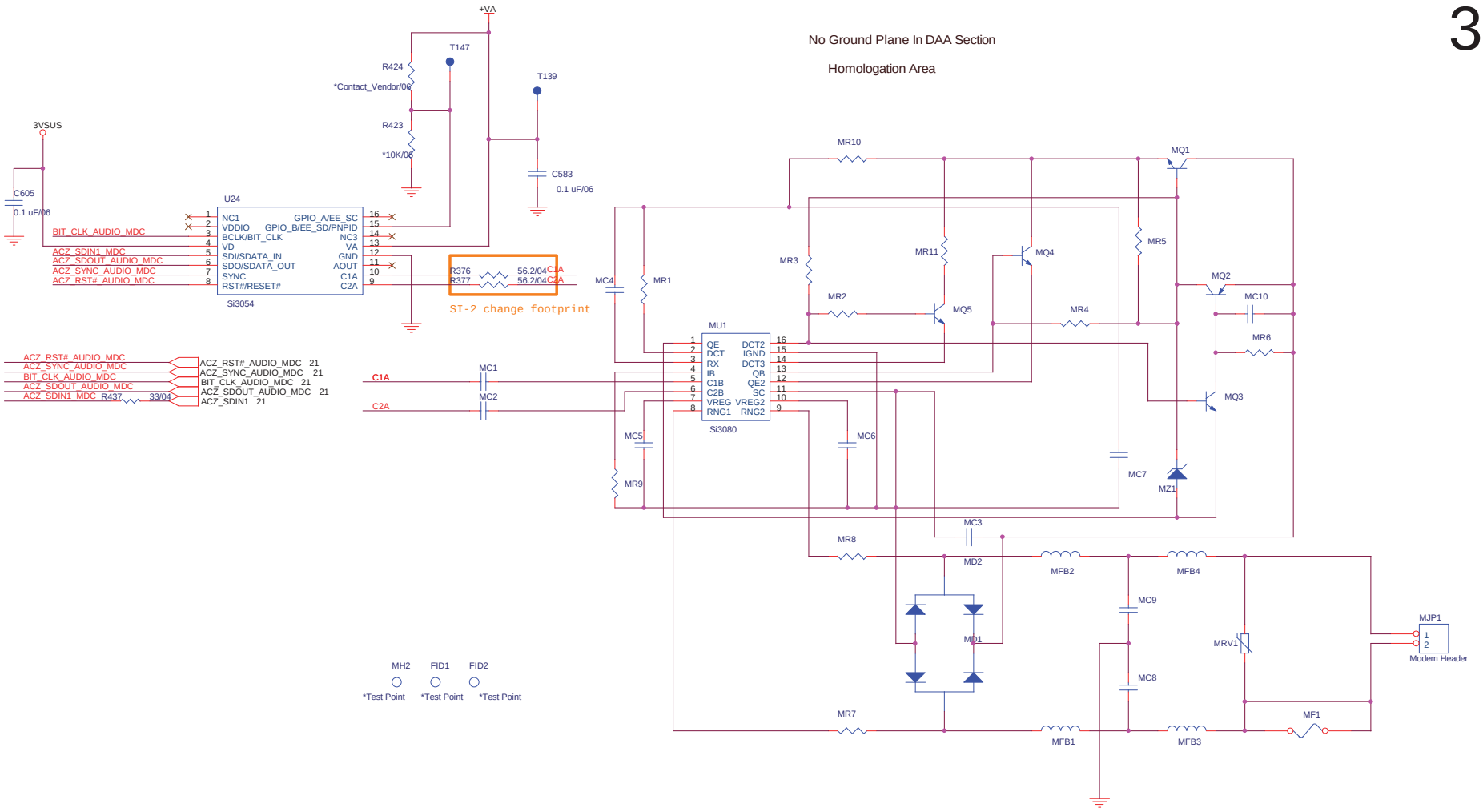
QFN20-4X4-5-25P

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 30 of 48

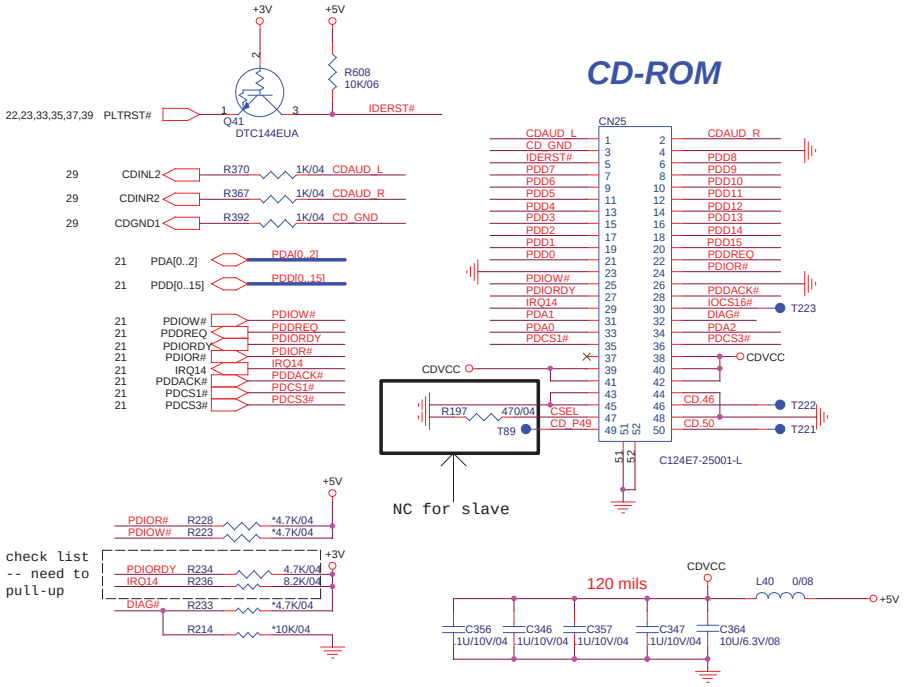


DESIGN SUBJECT TO CHANGE

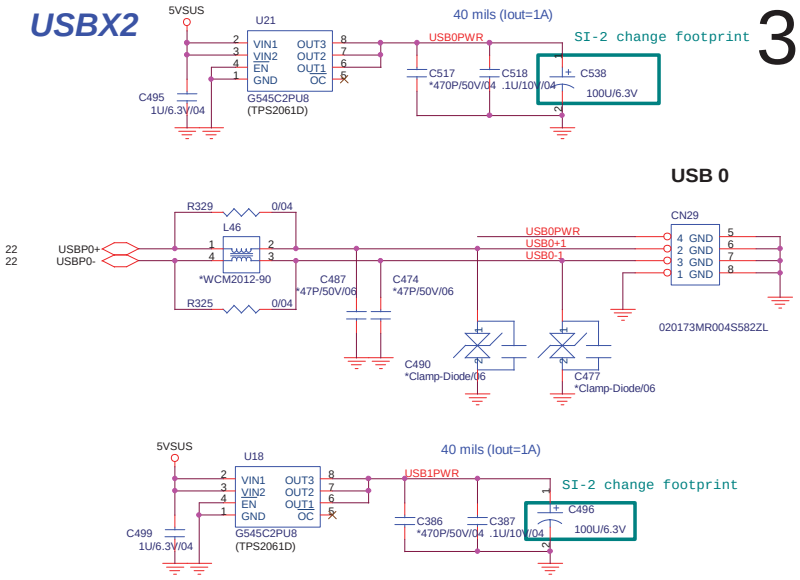
SILICON LABORATORIES CONFIDENTIAL

NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: MODEM(DAA)	Rev: 1A
Date: Monday, March 19, 2007	Sheet 31 of 48	

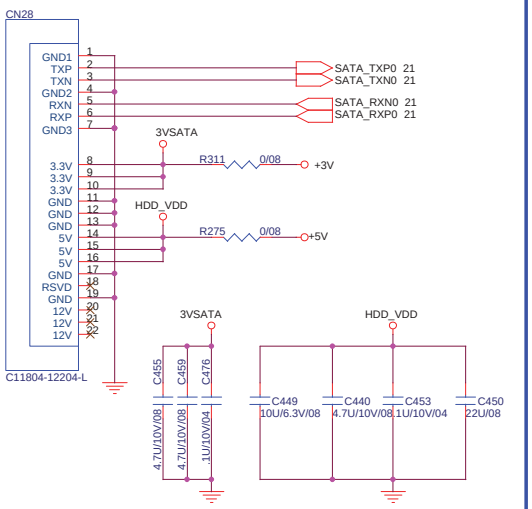
CD-ROM



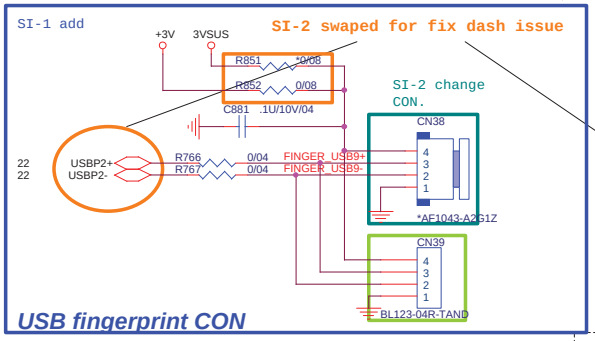
USBX2



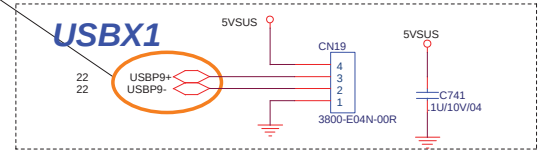
SATA_1 CONNECTOR



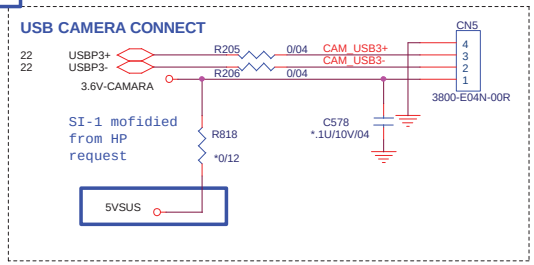
USB fingerprint CON

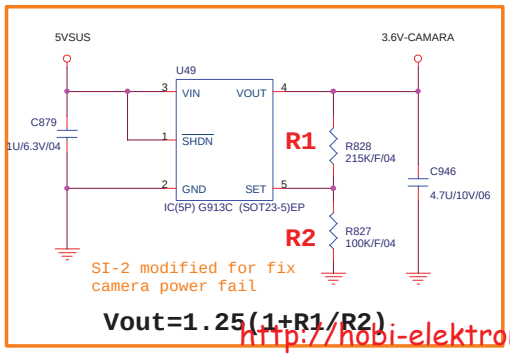


USBX1



USB CAMERA CONNECT





NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

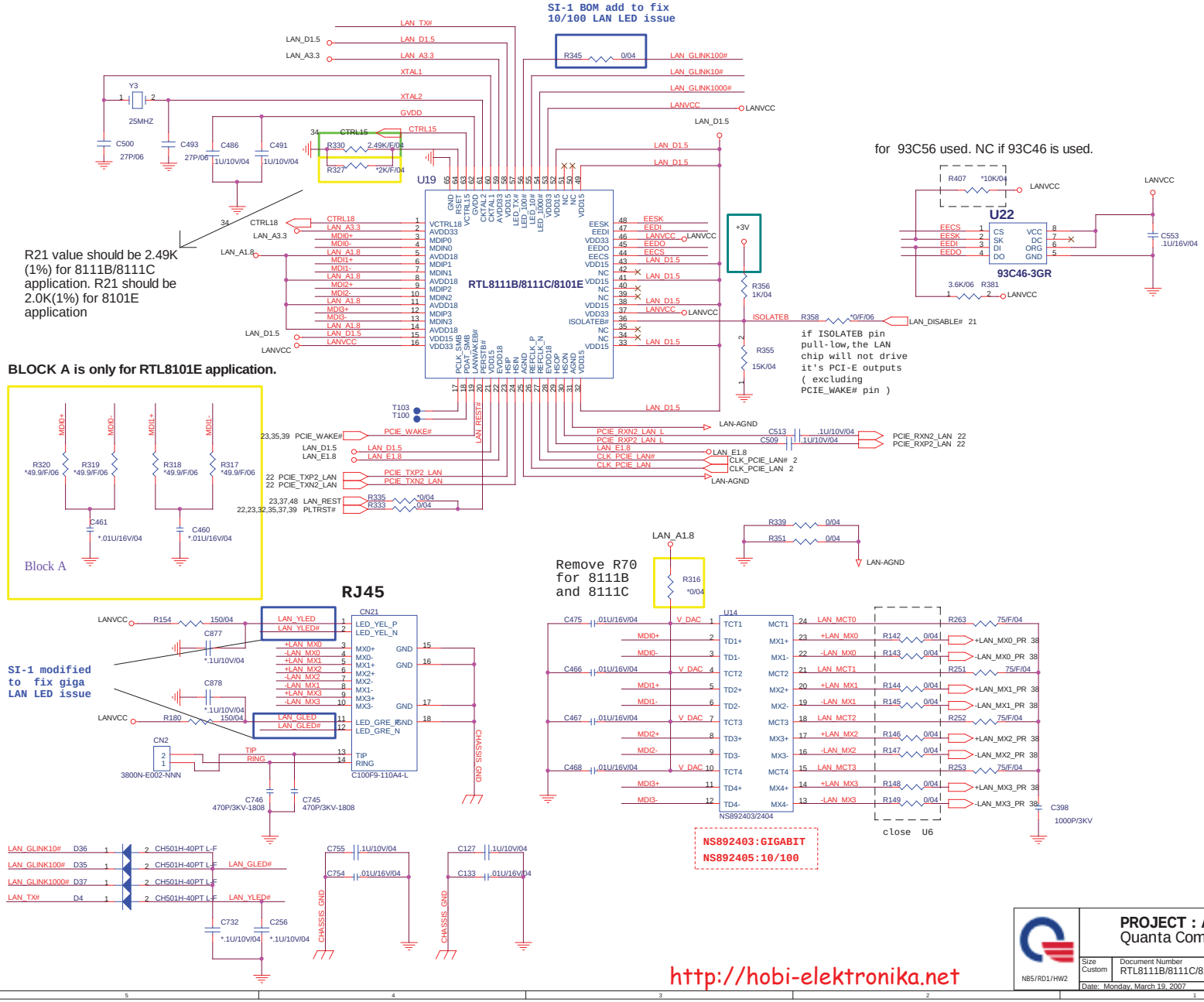
Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A
Date: Monday, March 19, 2007	Sheet 32 of 48	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

SI-1 BOM add to fix
10/100 LAN LED issue



for 93C56 used. NC if 93C46 is used.

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

BLOCK A is only for RTL8101E application.

RJ45

SI-1 modified
to fix giga
LAN LED issue

Remove R70
for 8111B
and 8111C

NS892403:GIGABIT
NS892405:10/100

PROJECT : AT5
Quanta Computer Inc.

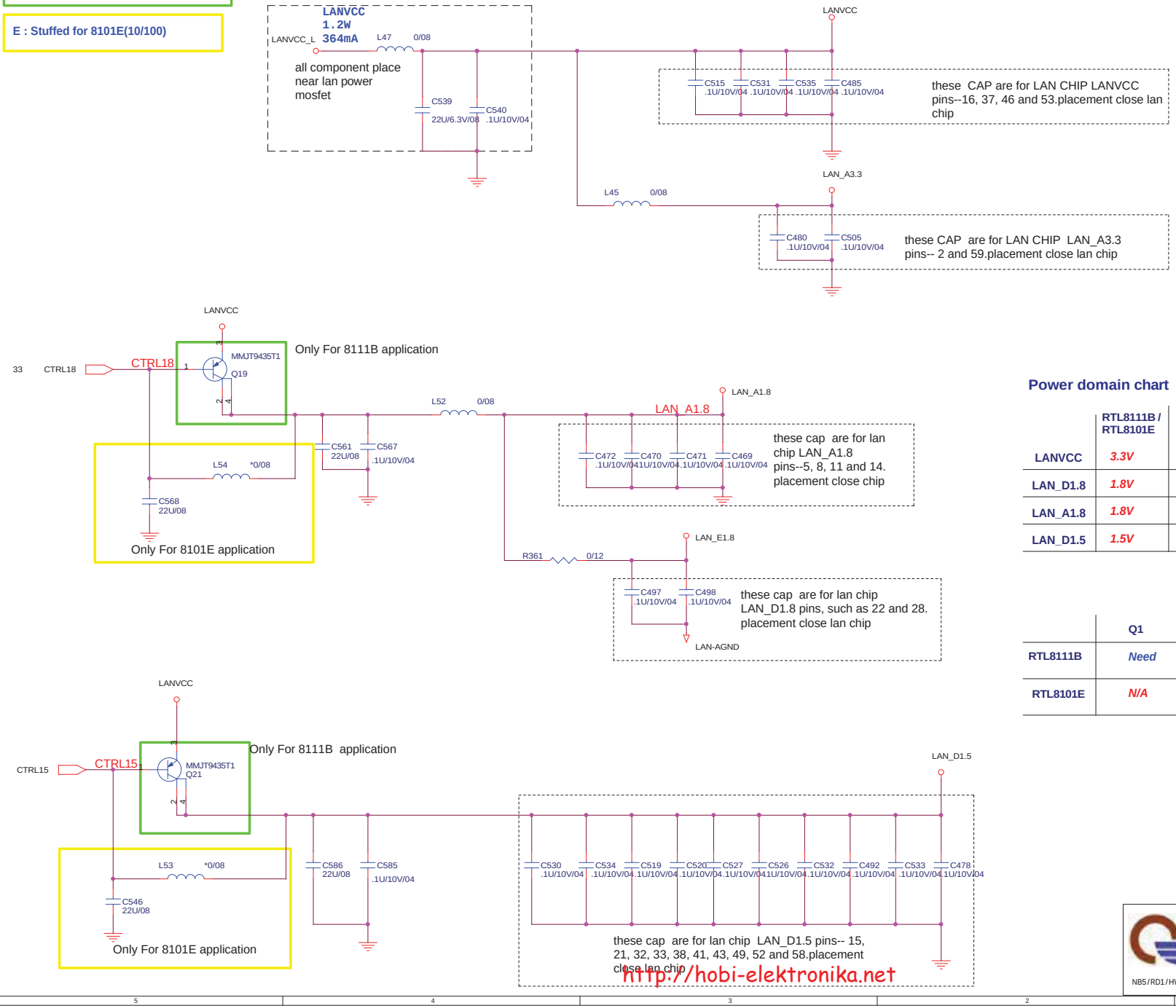
Size	Document Number	Rev
Custom	RTL8111B/8111C/8101E	1A

NB5/RD1/HW2

Date: Monday, March 19, 2007 Sheet 33 of 48

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A

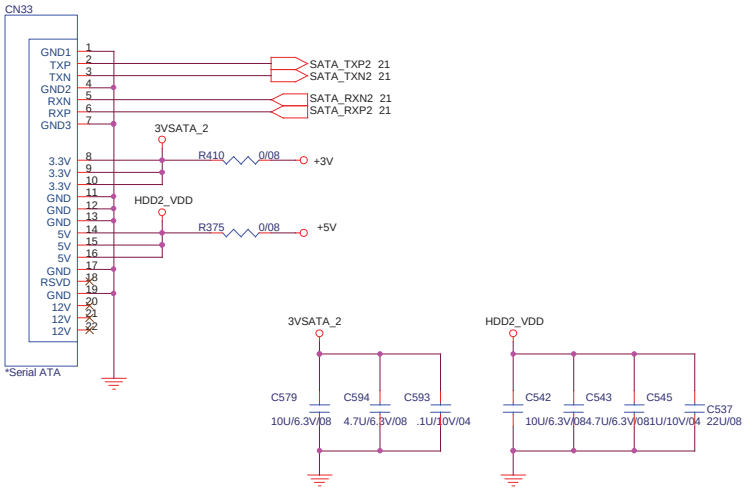
NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

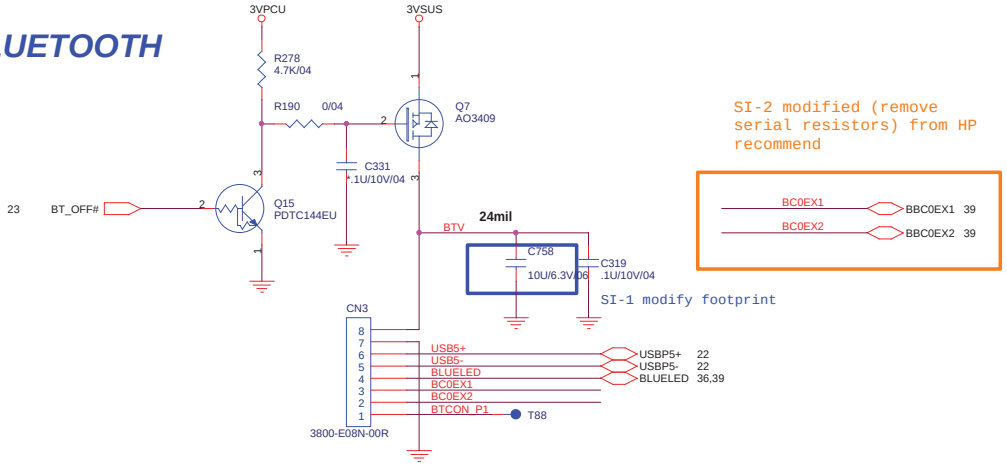
Size	Document Number	Rev
A3	LAN POWER	1A

Date: Monday, March 19, 2007 Sheet 34 of 48

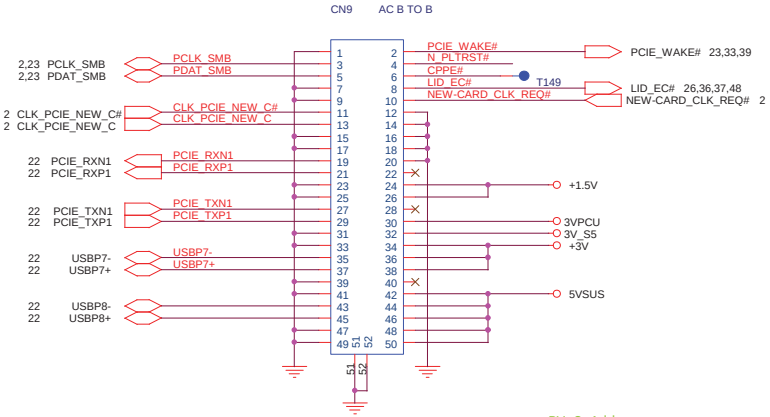
SATA_2 CONNECTOR
For 17"W Second HDD



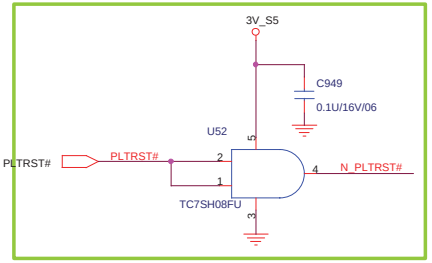
BLUETOOTH

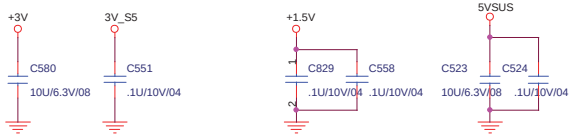


NEWCARD

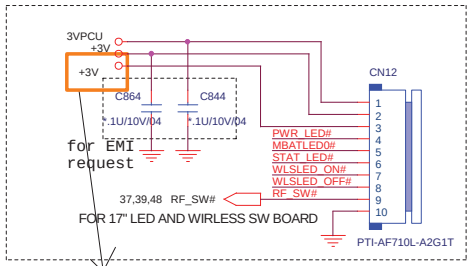


PV-2 Add

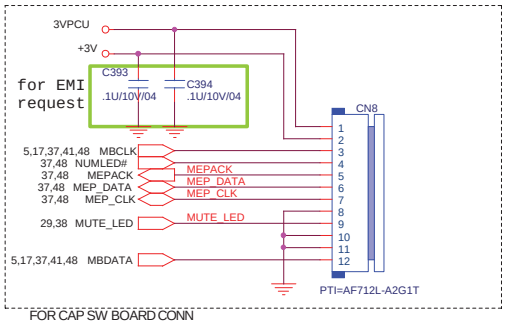


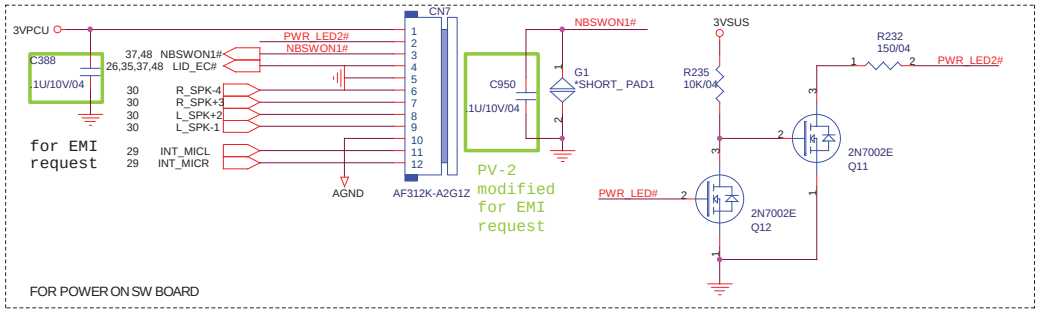


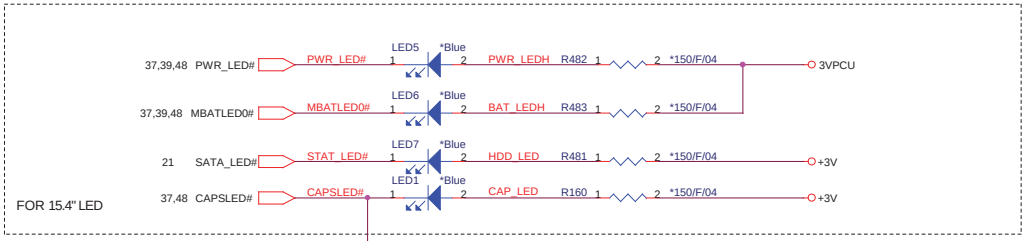
NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: NEW CARD/BT	Rev: 1A
Date: Monday, March 19, 2007	Sheet 35 of 48	

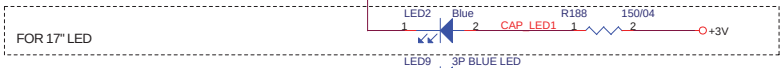


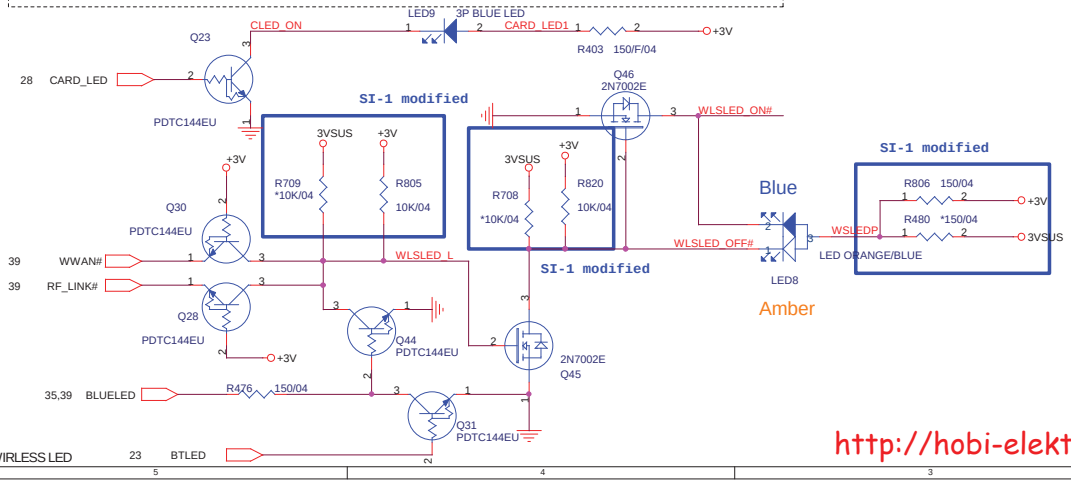
SI-2 modified for fix s3 not support wirless LED

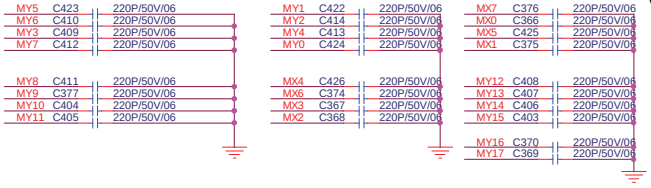




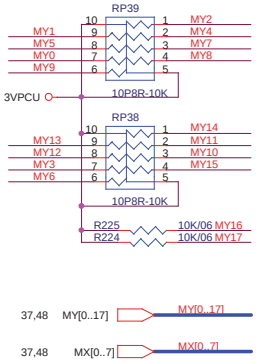


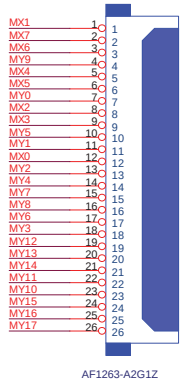


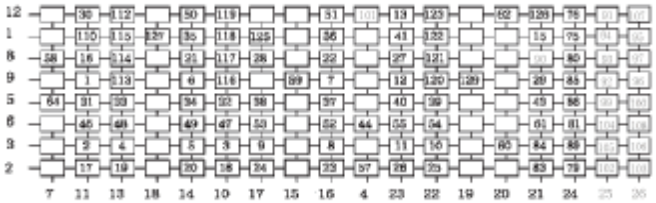




KEYBOARD PULL-UP







NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: LED/KEYBOARD/SW	Rev: 1A
Date: Monday, March 19, 2007	Sheet 36 of 48	

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

SI-1 DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

SI-1 modify (remove R245 and add R241)

SI-1 modify

SI-2 modified remove ISA BIOS

SELECT KBC TPYE

PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified remove ISA BIOS

TOUCH PAD CONNECTOR

25 mils

for EMI request

close conn

FOR 15.4"

FOR 17"

SI-1 ADD

PV-2 Add

ICH8 has internal pull-up

1M byte SPI BIOS

PROJECT : AT5
Quanta Computer Inc.

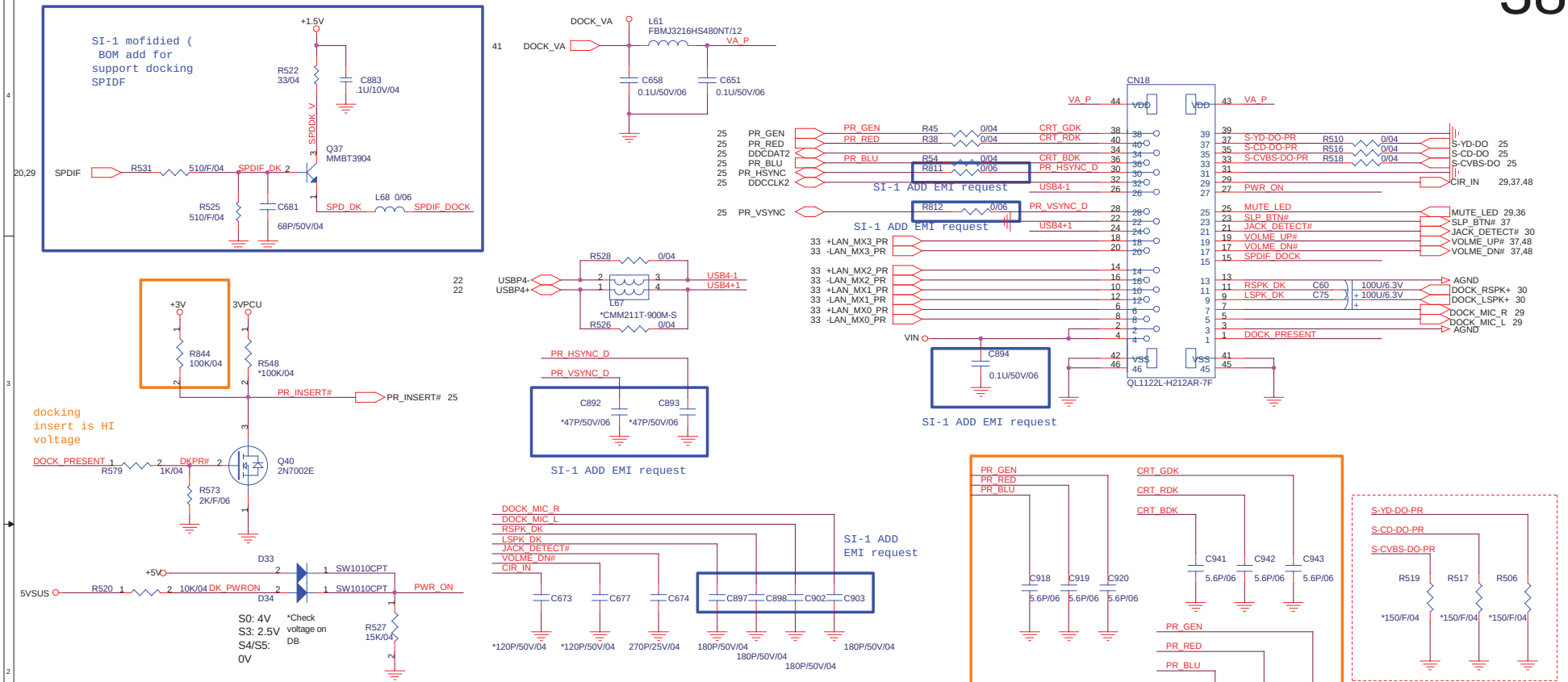
Size	Document Number	Rev
Custom	KB3920/ROM/TP	1A

N85/RD1/HW2

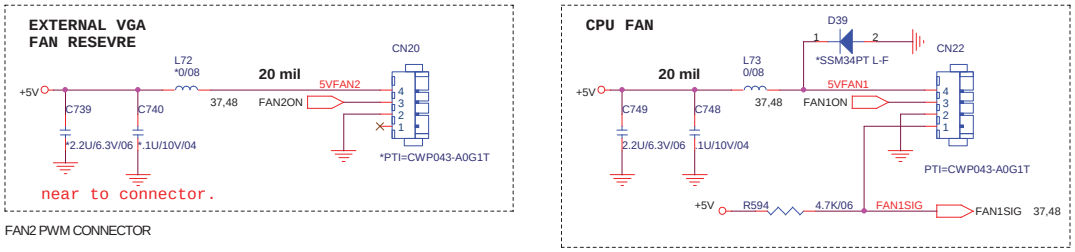
Date: Monday, March 19, 2007 Sheet 37 of 48

CABLE DOCK

support 6A 200mils
CX000480005



FAN



FAN2 PWM CONNECTOR

FAN1 PWM CONNECTOR

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Size: Custom	Document Number: CABLE DOCKING/FAN	Rev: 1A
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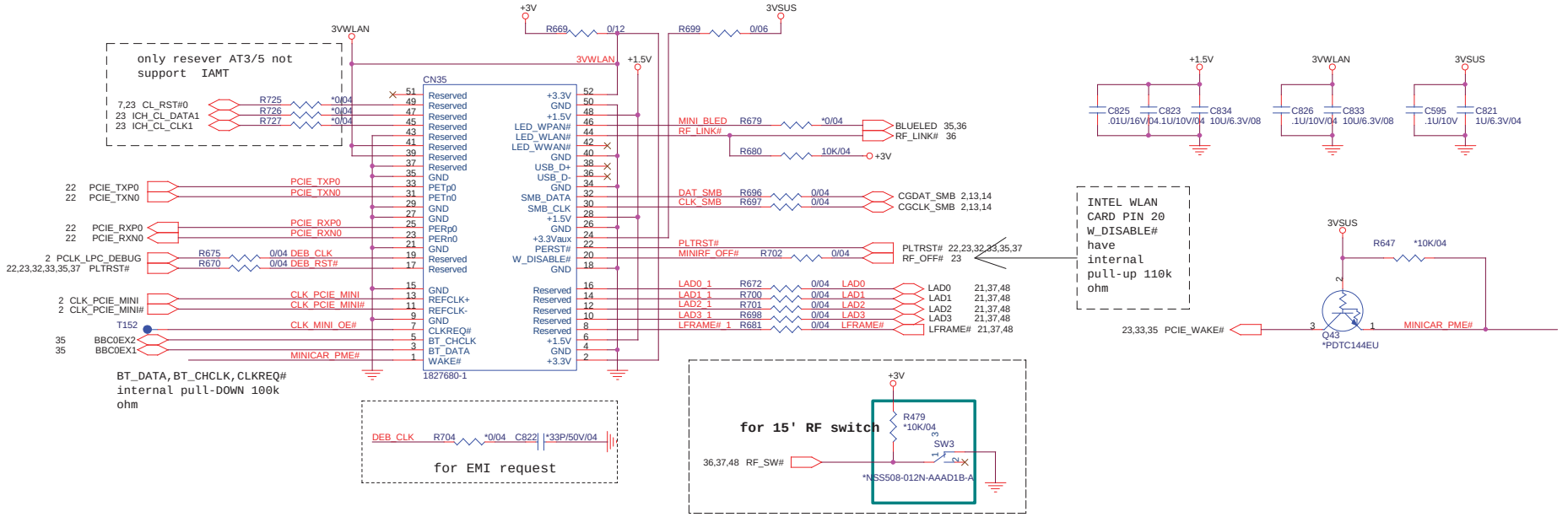
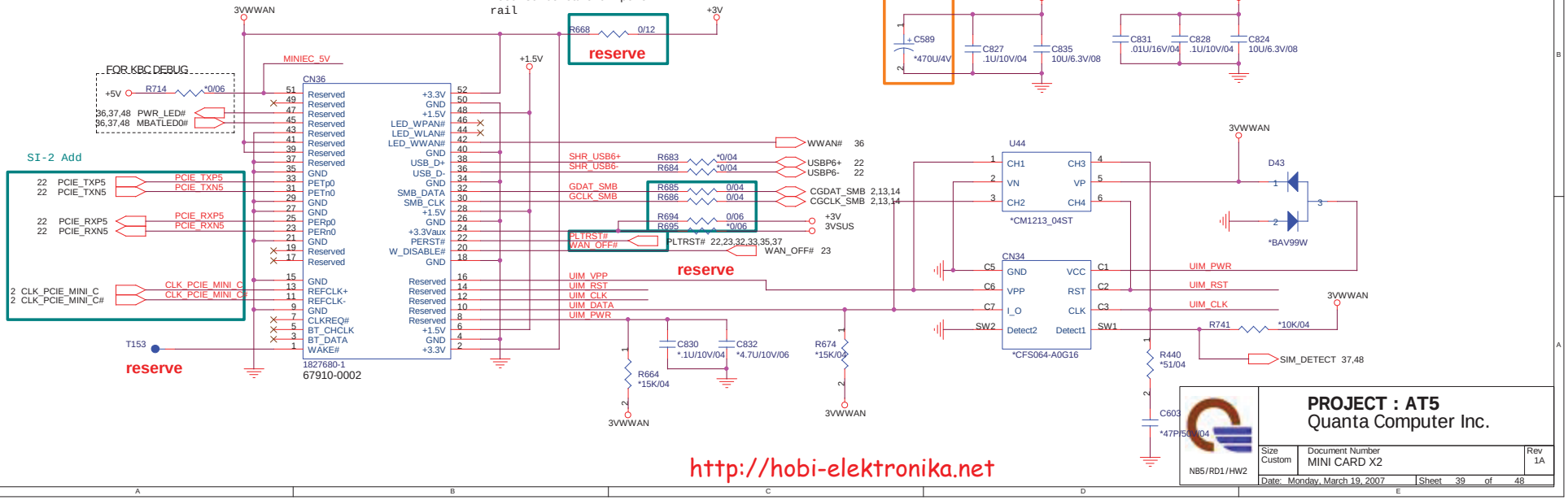
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

SI-2 modified (BOM remove C589)



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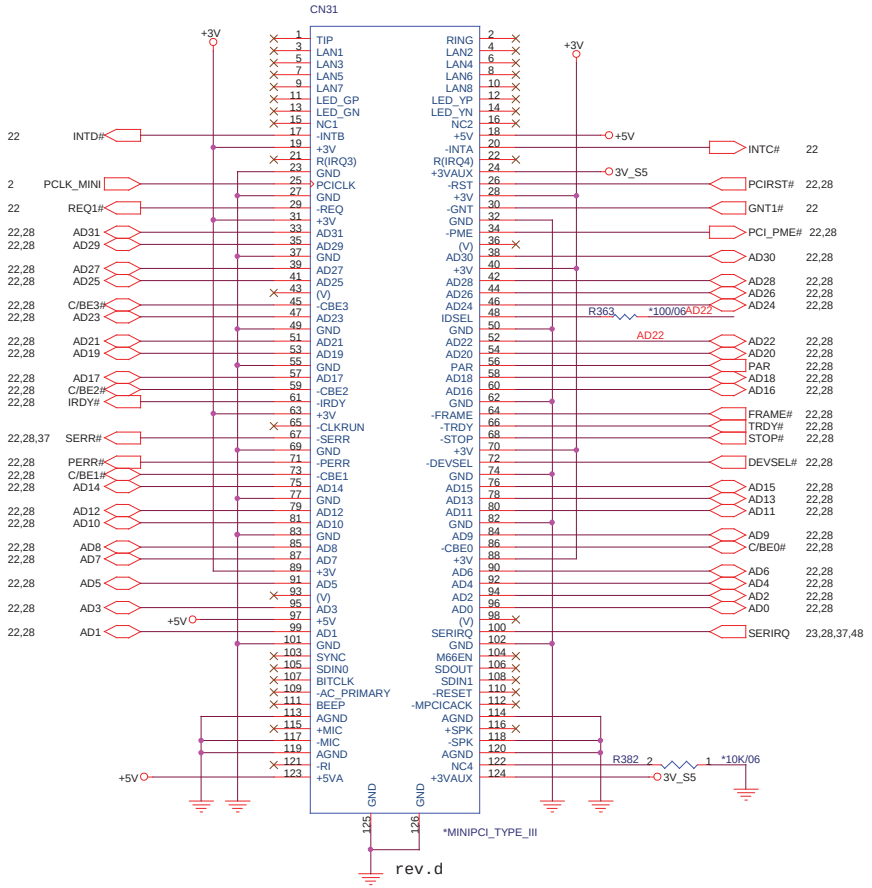
NB5/RD1/HW2

MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCI TYPE III SLOT	Rev: 1A
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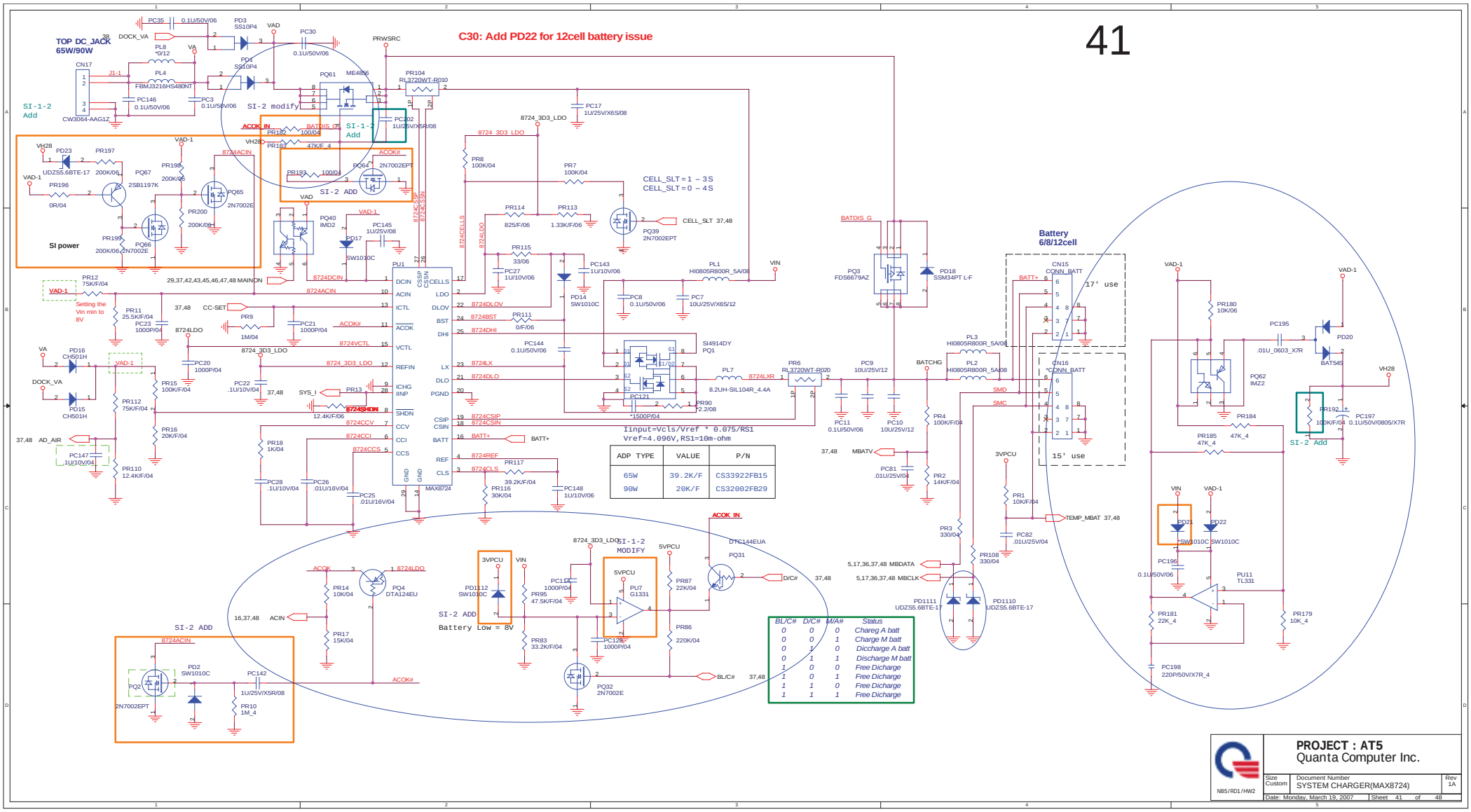

ADP TYPE	VALUE	P/N
65W	39.2K/F	CS33922FB15
90W	20K/F	CS32002FB29

BL/C#	D/C#	M/A#	Status
0	0	0	Chareg A batt
0	0	1	Charge M batt
0	1	0	Diccharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Rds(on) 13m ohm

Rds(on) 15m ohm

Max Power Consumption 1.6W

For G73 Only

SI-1 MODIFY

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Quanta Computer Inc.		
N85/RD1/HW2	Size: Custom	Document Number: 3v/5v
	Rev: 1A	
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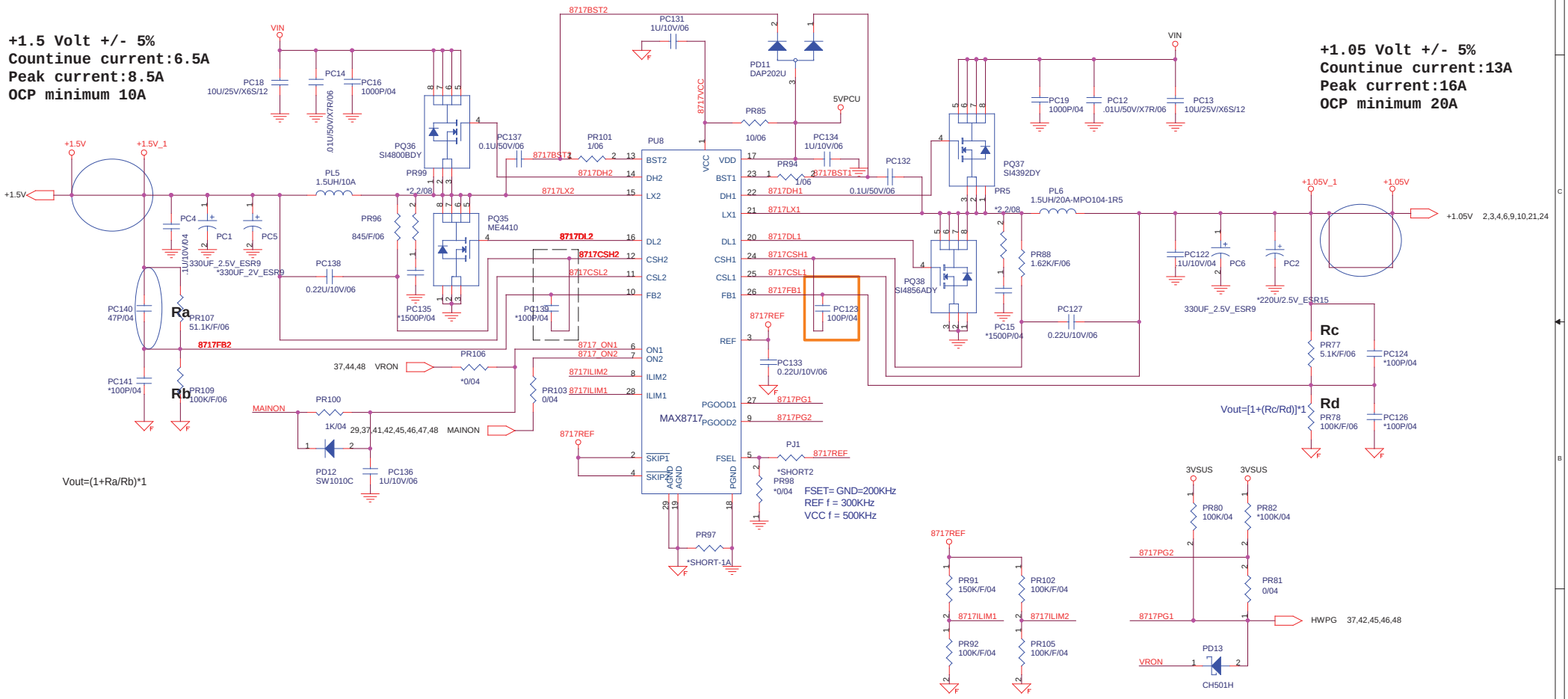
+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A

+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A



NB5/RD1/HW2	**PROJECT : AT5** Quanta Computer Inc.	
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
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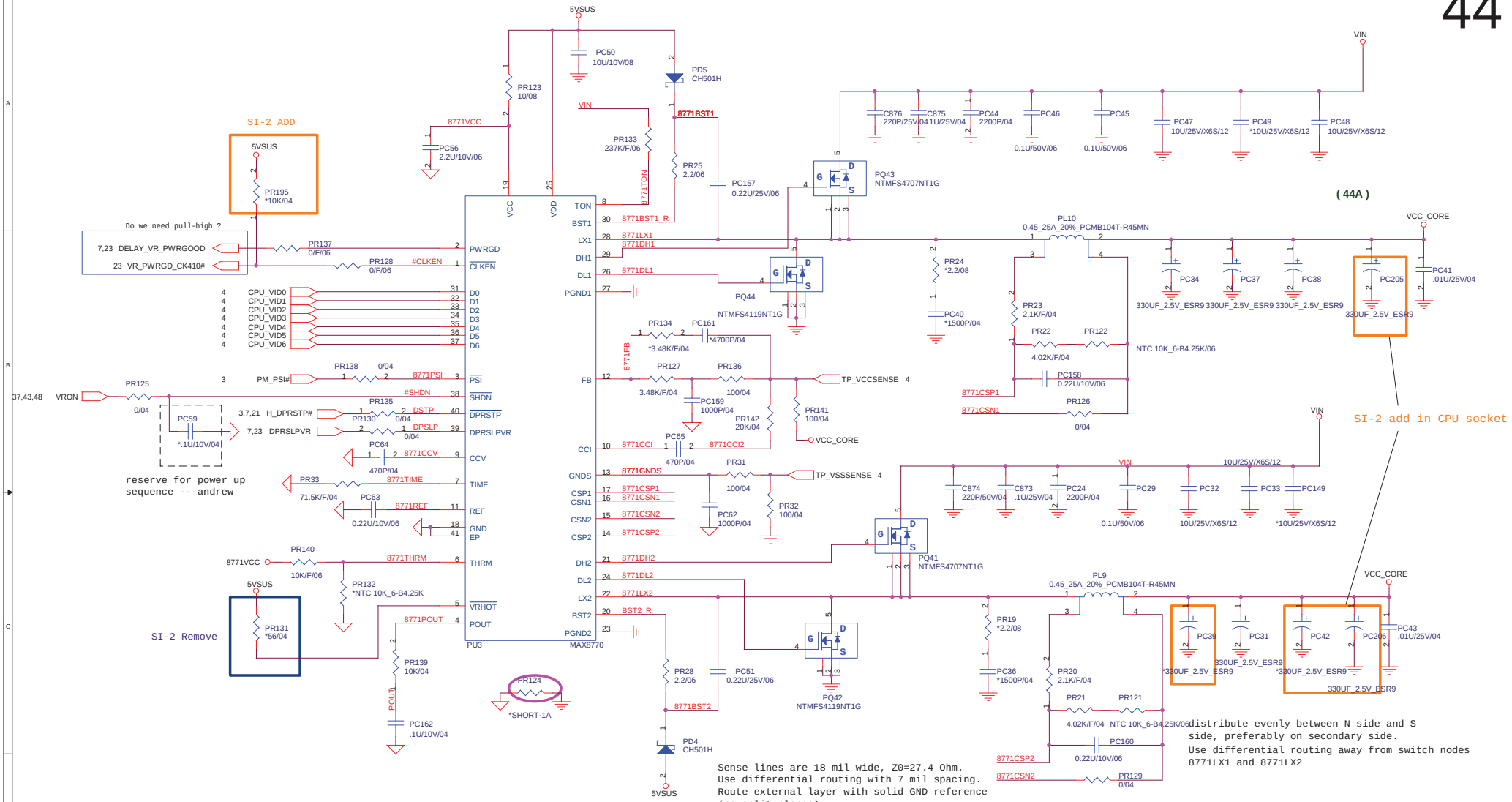

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
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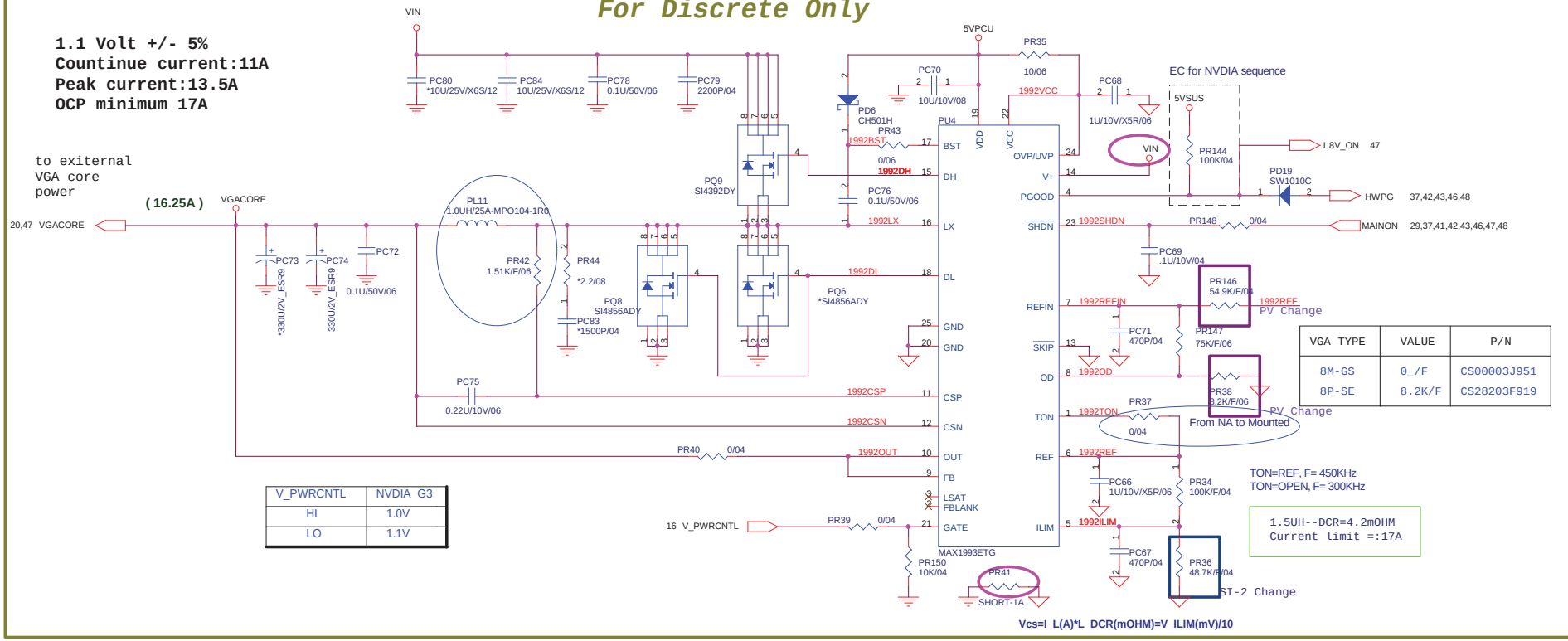
For Discrete Only

1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A

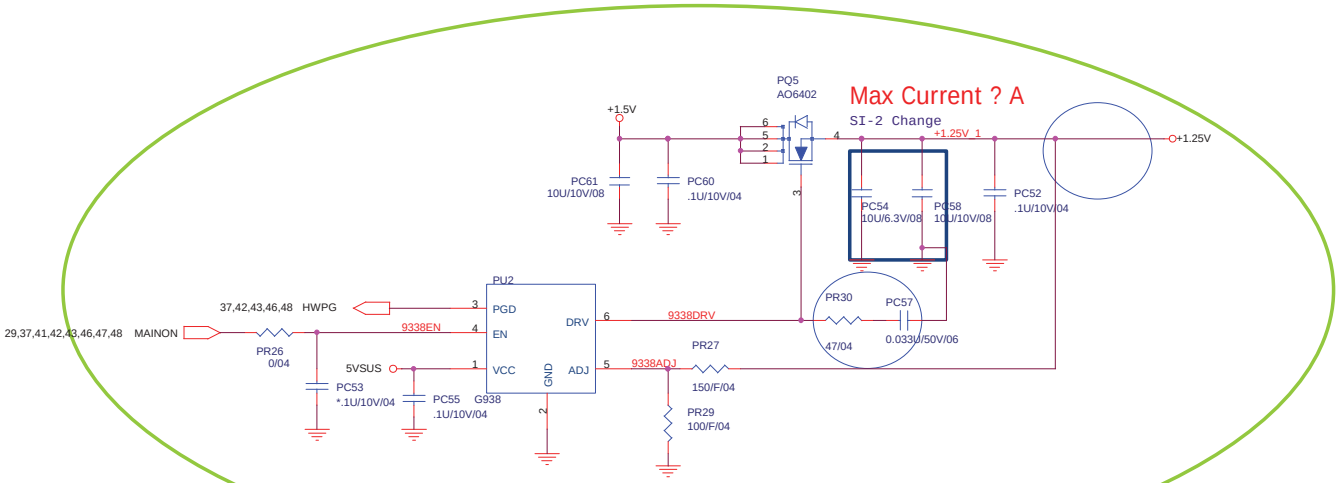
to exiternal
VGA core
power



V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

VGA TYPE	VALUE	P/N
8M-GS	0_/F	CS00003J951
8P-SE	8.2K/F	CS28203F919

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10



Vout1=(1+R1/R2)*0.5

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Quanta Computer Inc.

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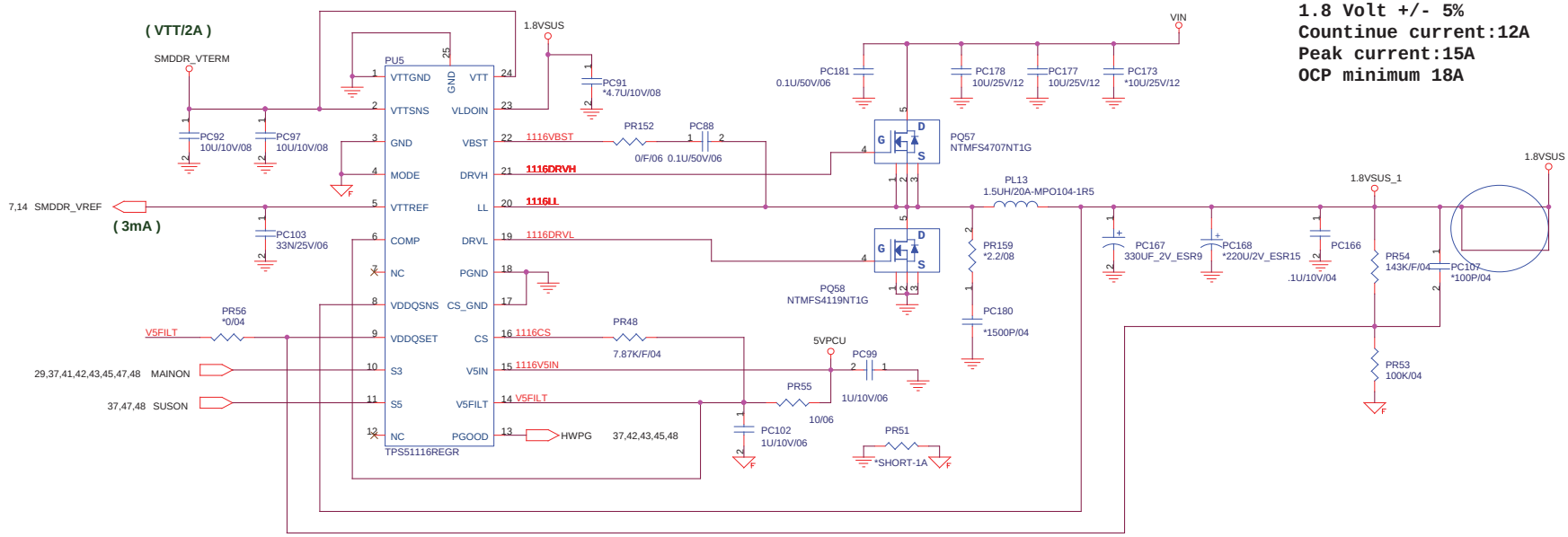
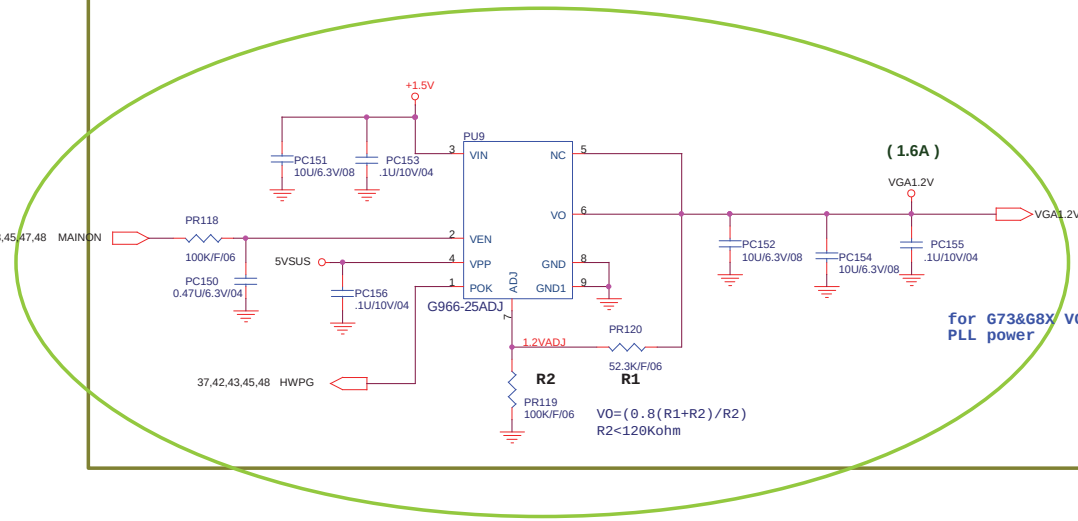
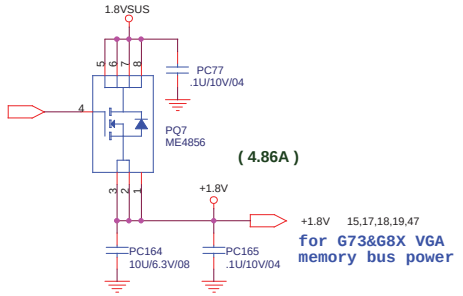
NB5/RD1/HW2



1.8 Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

For Discrete Only





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NB5/RD1/HW2

PROJECT : AT5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII 1.8VSUS/SMDDR_VTERM	1A

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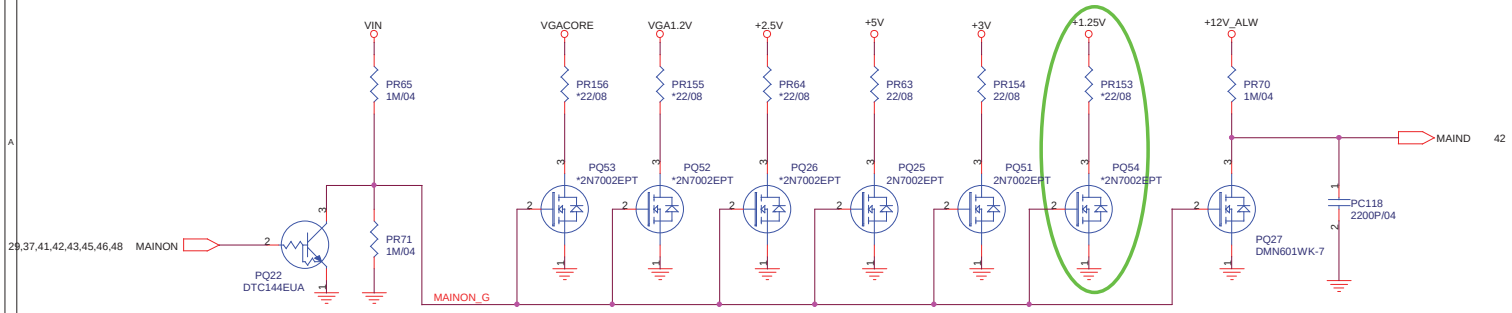

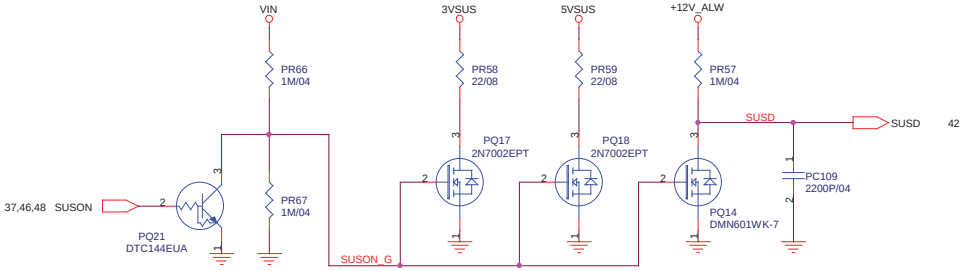

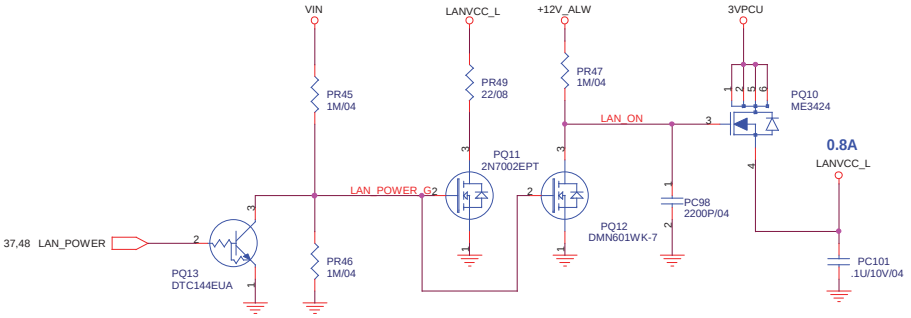

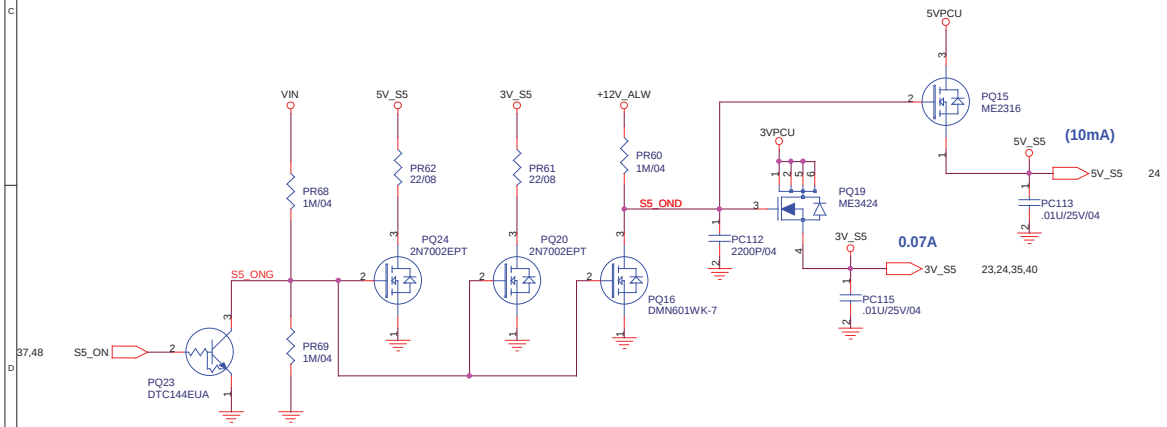

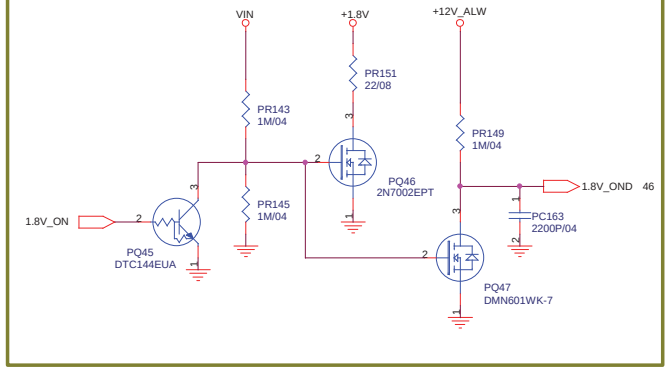

NB5/RD1/HW2	PROJECT : AT5 Quanta Computer Inc.	
Size: Custom	Document Number: DISCHARGE	Rev: 1A
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